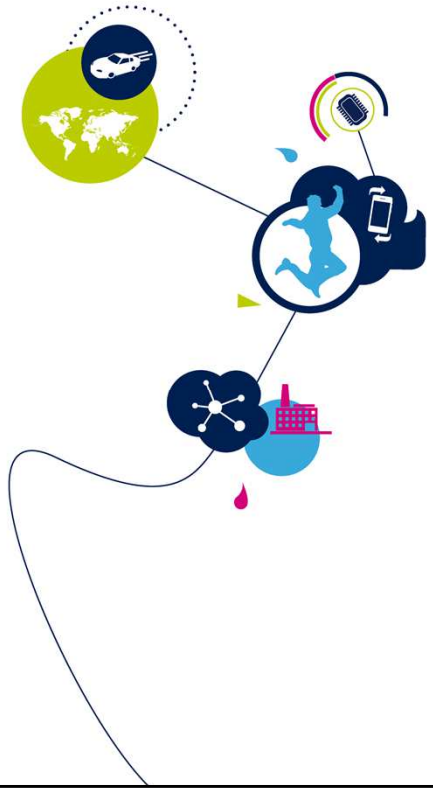
STM32L4+ vs STM32L4

Revision 2.0



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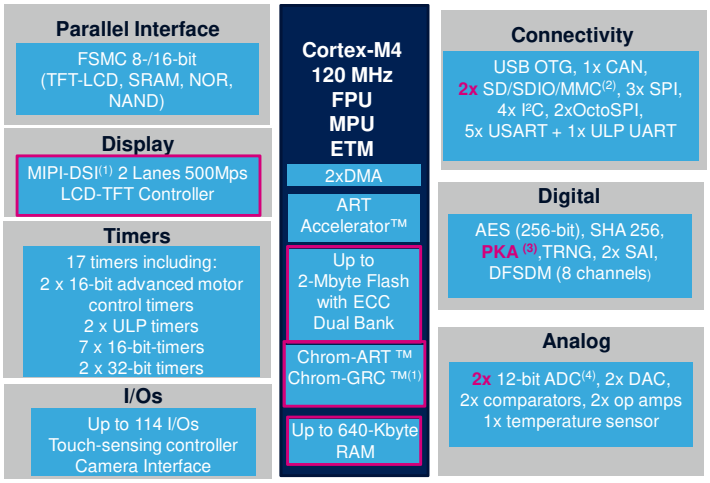
This module presentation presents the key differences between the STM32L4+ and the STM32L476/L486 devices.

STM32L4Rxxx/Sxxx and STM32L4P5xx/Q5xx Block Diagram

- Up to 120MHz, 406 CoreMark
- Up to 2MB Flash / 640KB SRAM for STM32L4Rxxx/Sxxx devices
- Up to 1MB Flash / 320KB SRAM for STM32L4P5xx/Q5xx devices
- MIPI-DSI 2 Lanes
- LCD-TFT controller
- Chrom-ART
- Chrom-GRC
- 2xOctoSPI



(1) MIPI-DSI and Chrom-GRC are available only on STM32L4Rxxx/Sxxx devices
(2) 2x SDMMC for STM32L4P5xx/Q5xx devices and 1x SDMMC for STM32L4Rxxx/Sxxx devices
(3) PKA only for STM32L4P5xx/Q5xx devices
(4) 2x ADC for STM32L4P5xx/Q5xx devices and 1x ADC for STM32L4Rxxx/Sxxx devices

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The STM32L4+ series stretches the STM32L4 technology by offering higher performance, that is to say 120 MHz/406 CoreMark executing from internal Flash memory

The new STM32L4+ embeds up to 2 Mbytes of dual-bank Flash memory and up to 640 Kbytes of embedded SRAM.

It also embeds advanced graphic features enabling state-of-the-art Graphic User Interfaces.:

- The Chrom-ART Accelerator™, the ST proprietary 2D hardware graphic accelerator, efficiently handles repetitive graphic operations releasing the main CPU capabilities for real-time processing or even more

advanced graphic operations.

- The Chrom-GRC™ round display memory optimizer, allowing up to 20% of graphic resources optimization

- The LCD-TFT controller and MIPI DSI controller supporting 2 lanes.

- 2 x Octo SPI supporting Flash and PSRAM memories.

The system frequency is increased up to 120 MHz while keeping state of the art ultra-low power figures.

STM32L4+ & STM32L4 Series Pin Compatibility

Package	STM32L4P5xx/Q5xx vs. STM32L4R5xx/S5xx/R7xx/S7xx	STM32L4P5xx/Q5xx vs. STM32L4R9xx/S9xx	STM32L4P5xx/Q5xx vs. STM32L4 Series	STM32L4R5xx/S5xx/R7xx/S7xx vs. STM32L4 Series	STM32L4R9xx/S9xx vs. STM32L4 Series
LQFP48 UFQFPN48 	-	-	compatible	-	-
LQFP64 	-	-	compatible	-	-
LQFP100 	compatible	incompatible	compatible	compatible	incompatible
WLCSP100 	-	-	compatible	-	-
UFBGA132 	compatible	-	compatible	compatible	-
LQFP144 	compatible	incompatible	compatible	compatible	incompatible
WLCSP144 	-	-	-	-	-
UFBGA144 	-	-	-	-	incompatible
UFBGA169 	compatible	incompatible	compatible	compatible	incompatible

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For more details about pin to pin compatibility refer to **AN5017** "Migrating between STM32L476xx/486xx and STM32L4+ Series microcontrollers"

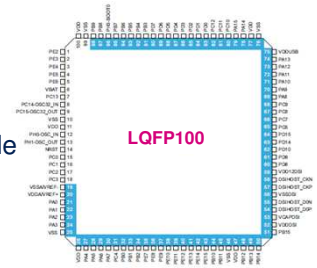
The STM32L4+ series is fully pin to pin compatible with the STM32L4 series except for the STM32L4R9xx/S9xx lines.

STM32L4+ & STM32L4 Series

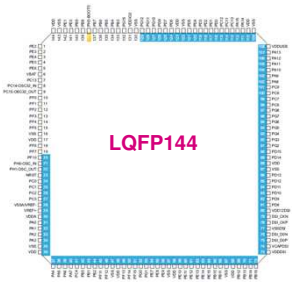
Pin Compatibility

- Pin difference notification for board design with STM32L4S9xx/4R9xx

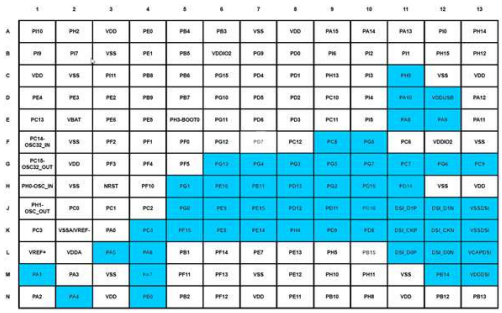
Pin 19 to pin 98
are not compatible



Pin 20 to pin 129
are not compatible



UFBGA169 Ball-out not compatible



Balls in Blue are
not compatible

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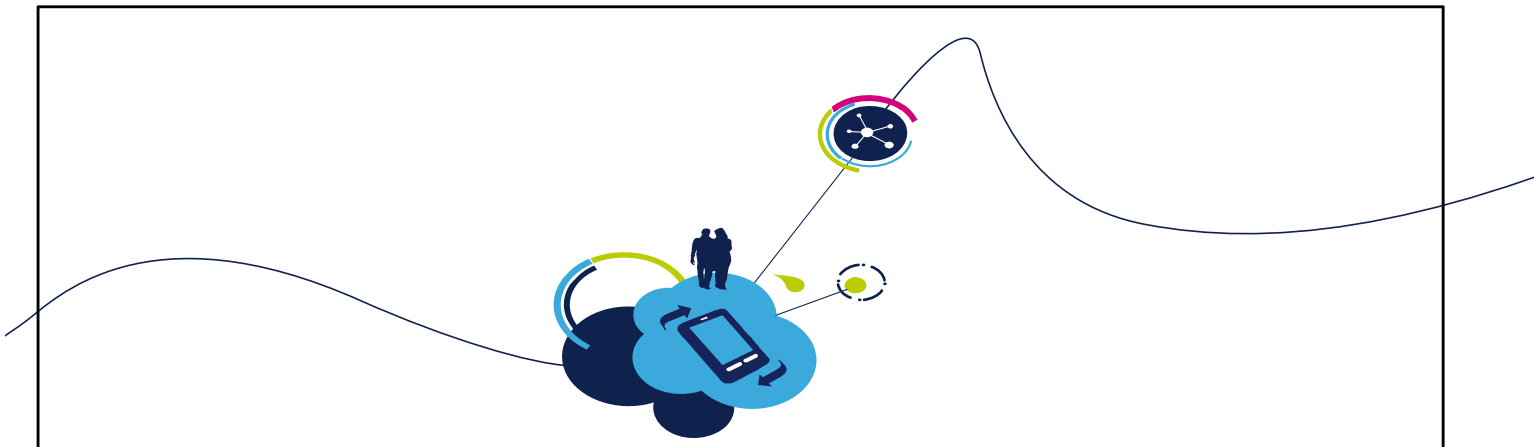
The three figures illustrate the LQFP100, LQFP144 and UFBGA169 pinout/ball-out differences between STM32L476/486, STM32L4Q5xx/P5xx and the STM32L4R9/4S9 lines.

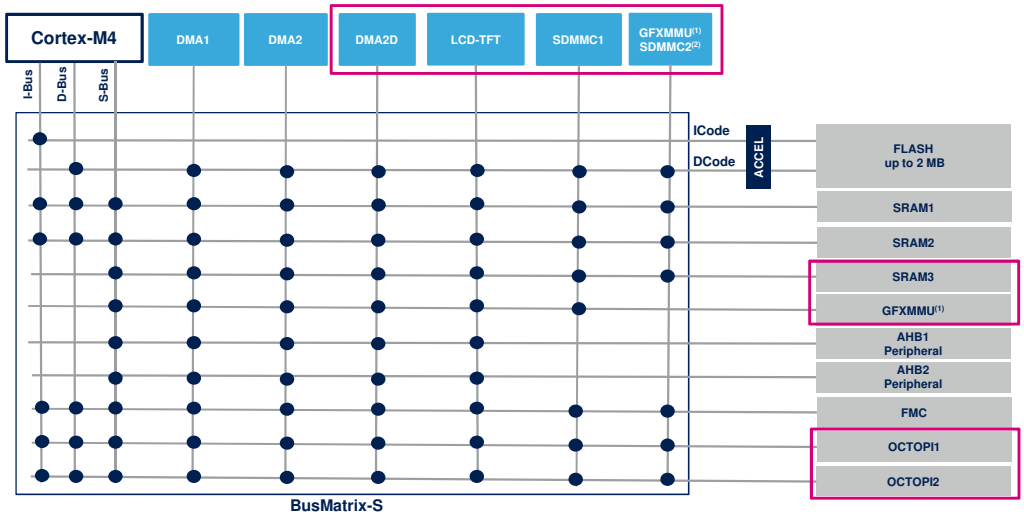


System Architecture

Let’s have a look at the System architecture changes that we see with the STM32L476/486 microcontrollers.

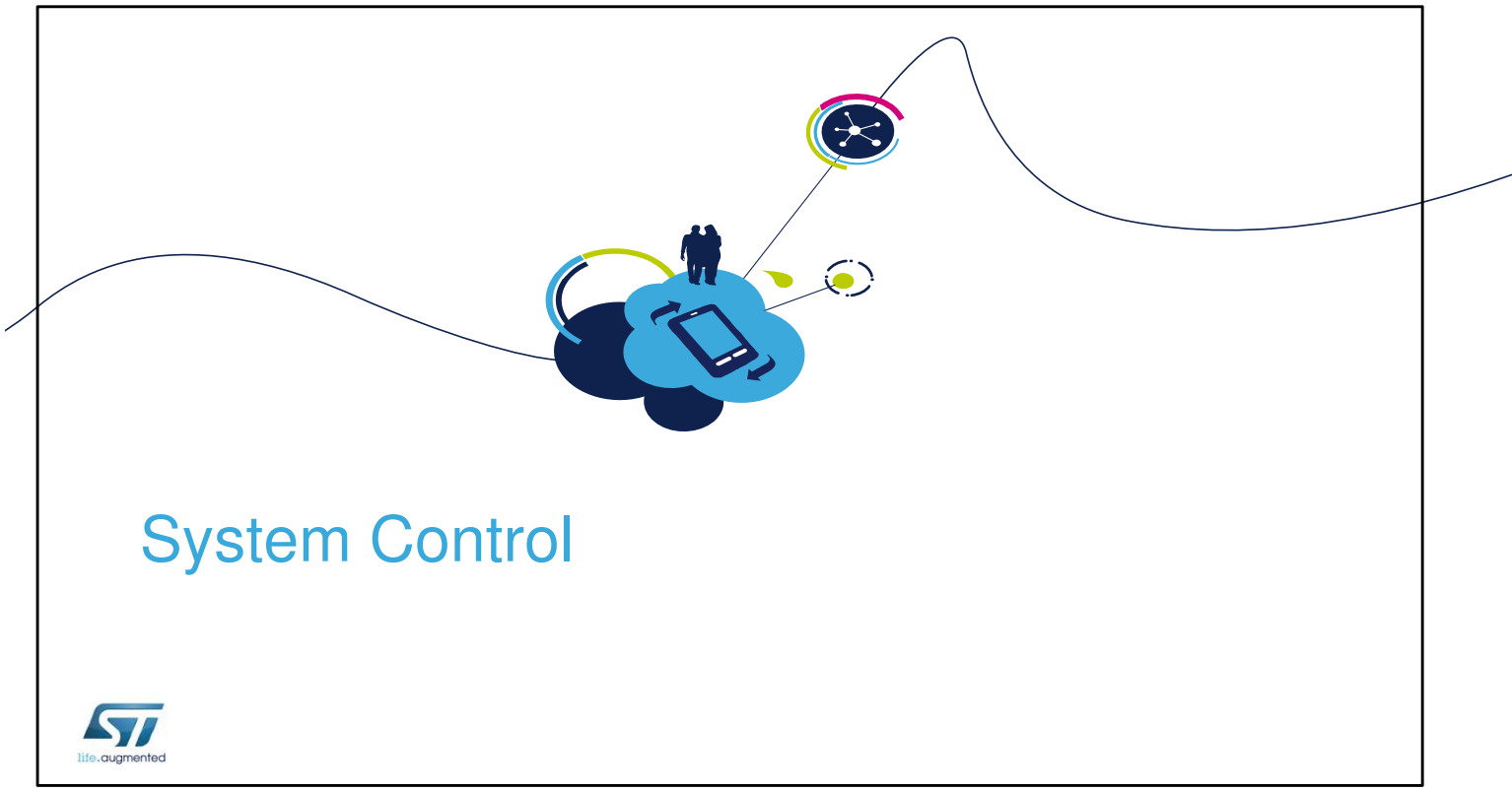
STM32L4+ System Architecture

32-bit multilayer AHB bus matrix, 9 Masters, 11 Slaves



(1) GFXMMU is only available on STM32L4P5xx/4Q5xx devices
(2) SDMMC2 is only available on STM32L4Rxxx/4Sxxx devices

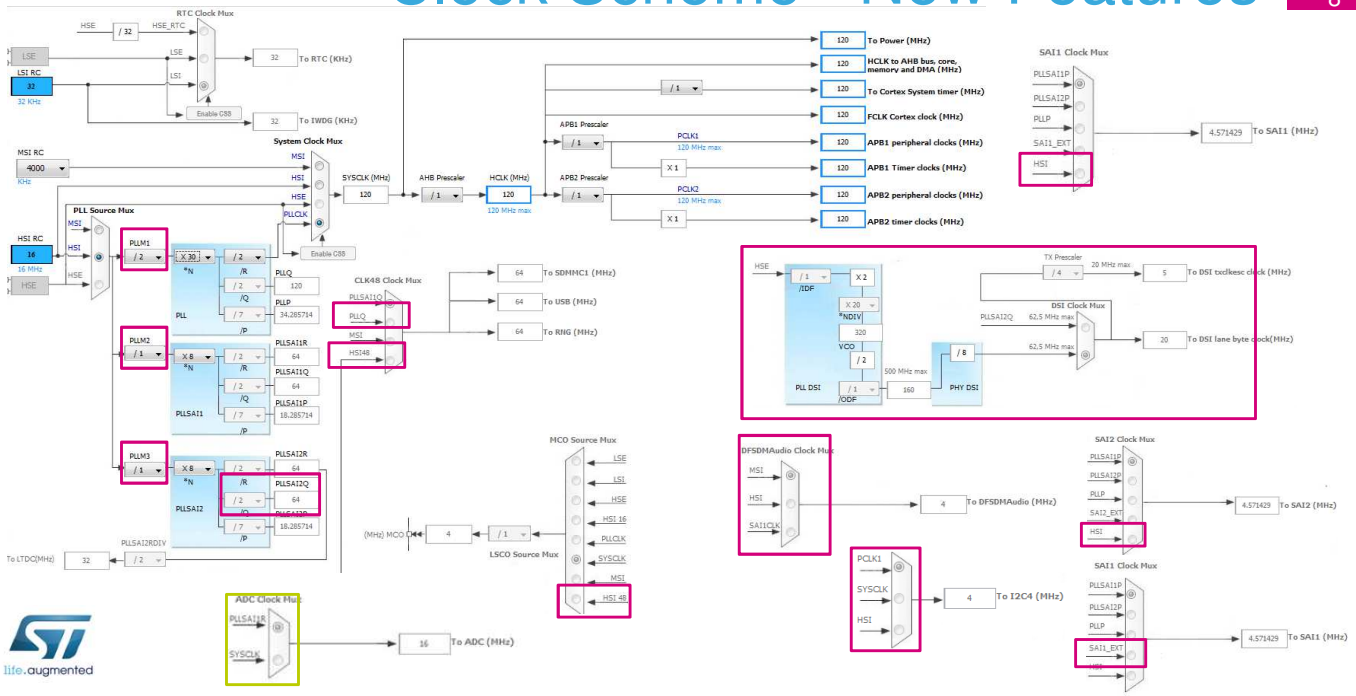
The STM32L4+ main system architecture consists of 32-bit multilayer AHB bus matrix that interconnects 9 masters and 11 slaves. The main differences with STM32L476/486 devices are highlighted in pink square.



System Control

The STM32L4+ brings some new features in clock configuration management.

Clock Scheme - New Features



The STM32L4+ series features additional clock configuration - the main differences with the STM32L476/486 devices are highlighted with the pink squares.

Clock Scheme New Features

	STM32L476xx/486xx	STM32L4+
PLLM divider	PLLM:1 to 8	PLLM: 1 to 16
PLLN factor	PLLN:8 to 86	PLLN: 8 to 127
PLLP divider	PLLP: 7 or 17	PLLP: 2 to 31
PLLSAI1M divider	NA	PLLSAI1M: 1 to 16
PLLSAI1N factor	PLLSAI1N: 8 to 86	PLLSAI1N: 8 to 127
PLLSAI1P divider	PLLSAI1P: 7 or 17	PLLPSAI1P: 2 to 31
PLLSAI2M divider	NA	PLLSAI2M: 1 to 16
PLLSAI2N factor	PLLSAI2N: 8 to 86	PLLSAI2N: 8 to 127
PLLSAI2P divider	PLLSAI2P: 7 or 17	PLLSAI2P: 2 to 31
PLLSAI2Q divider	NA	PLLSAI2Q: 2, 4, 6 or 8
HSI16	HSITRIM[4:0]	HSITRIM[6:0]
HSI48	NA	RC with clock recovery used for USB/RNG/SDMMC

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This table highlights the differences related to the Reset and Clock Control (RCC) mainly for PLL dividers and factors between STM32L4+ and STM32L476xx/486xx microcontrollers.

System Clock Selection

- Switching from Low to High speed or from High to Low speed system clock, it is recommended to use a transition state with a medium speed clock for at least 1us.
- Clock source switching conditions:
  - Switching from HSE or HSI or MSI to PLL with AHB frequency (HCLK) higher than 80MHz.
  - Switching from PLL with HCLK higher than 80MHz to HSE or HSI or MSI
- Transition state:
  - Set the AHB prescaler HPRE[3:0] bits to divide System frequency by 2
  - Switch system clock to PLL
  - Reconfigure AHB prescaler bits to needed HCLK frequency

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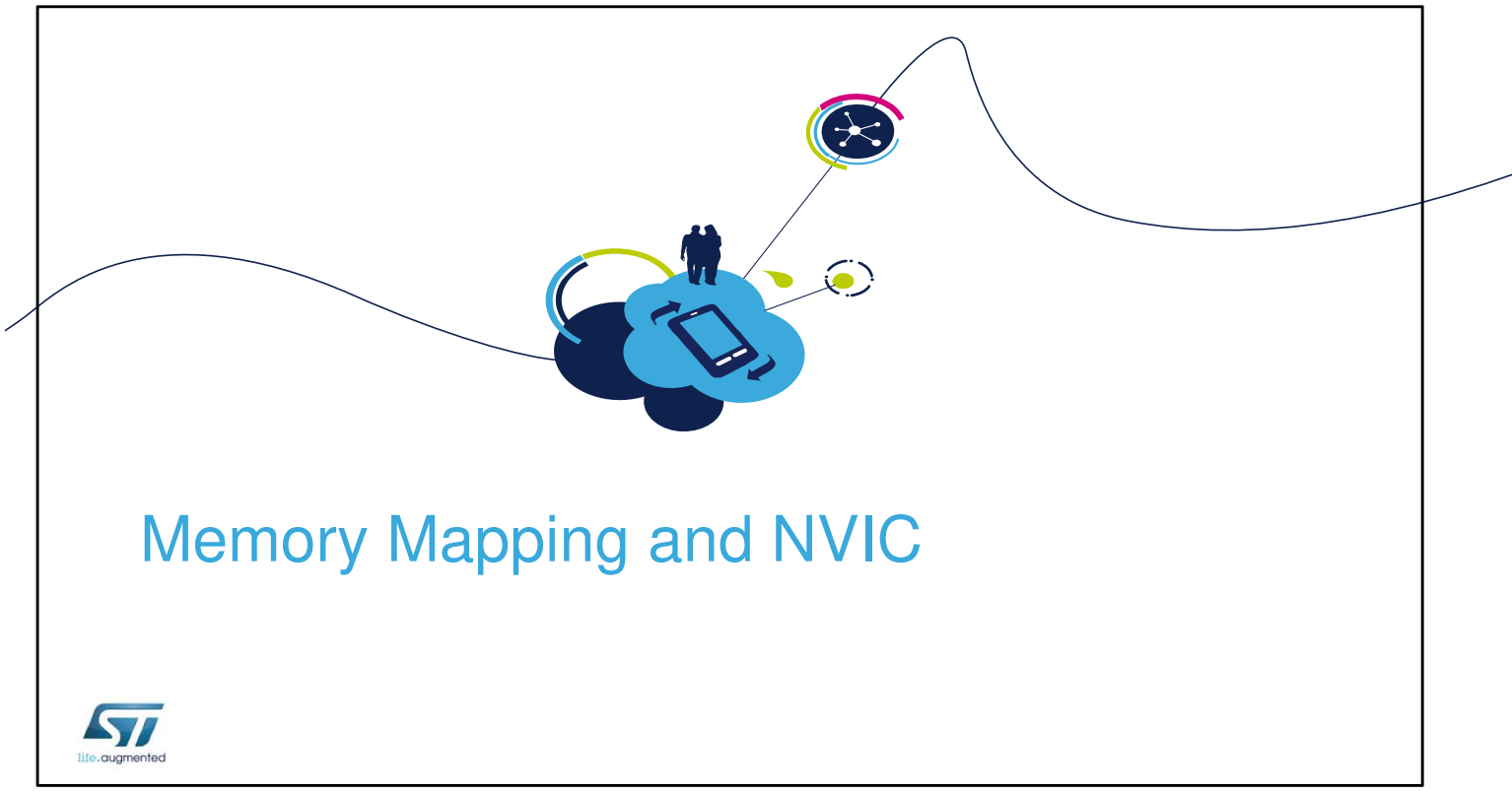
In STM32L4+ Series devices, it is recommended to use a transition state while switching from Low to High speed or from High to Low speed system clock. This slide presents the recommended sequence for the transition state.

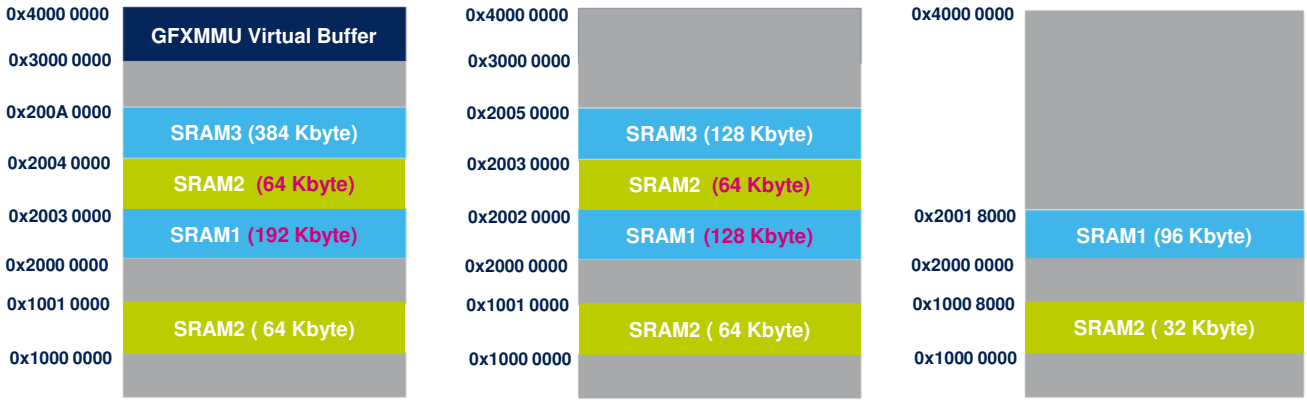


Memory Mapping and NVIC

These slides show the embedded SRAM memory mapping differences between STM32L4+ and STM32L476xx/486xx microcontrollers and the interrupt vector table as well.

Embedded SRAM Memory Mapping

- Up to 640KB, All SRAMs are contiguous



STM32L4Rxxx/4Sxxx
(640 Kbytes)

STM32L4P5xx/4Q5xx
(320 Kbytes)

STM32L476/L486
(128 Kbytes)

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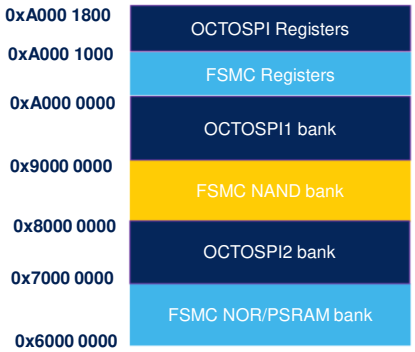
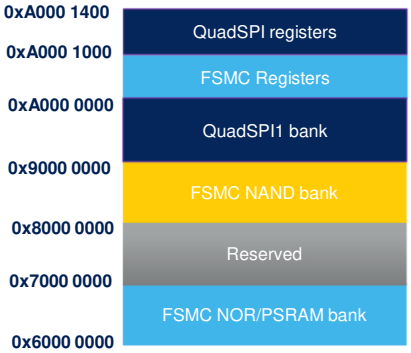
The STM32L4+ Series devices feature an additional SRAM3. Compared to STM32L476xx/486xx devices, the SRAM2 is contiguous to the SRAM1 and it is still mapped at 0x1000 0000 address.

External Memory Mapping



STM32L4+ Series



STM32L476/486

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This slide presents the external memory mapping differences between STM32L4+ Series and STM32L476xx/486xx devices.

NVIC Interrupt Vectors

Position	STM32L4Rxxx/4Sxxx	STM32L4P5xx/4Q5xx	STM32L476xx/486xx
18	ADC1	ADC1_2	ADC1_2
41	RTC_ALARM	RTC_ALARM_SSRU	RTC_ALARM
42	DFSDM1_FLT3	Reserved	DFSDM1_FLT3
47	Reserved	SDMMC2	ADC3
63	DFSDM1_FLT2	Reserved	DFSDM1_FLT2
71	OCTOSPI1		QUADSPI
76	OCTOSPI2		SWPMI
78	DSIHOST	Reserved	LCD
82	HASH and CRS		Reserved
83	I2C4_EV		Reserved
84	I2C4_ER		Reserved
85	DCMI	DCMI_PSSI	Reserved
90	DMA2D		Reserved
91	LCD-TFT		Reserved
92	LCD-TFT_ER		Reserved
93	GFXMMU	Reserved	Reserved
94	DMAMUX1_OVR		Reserved

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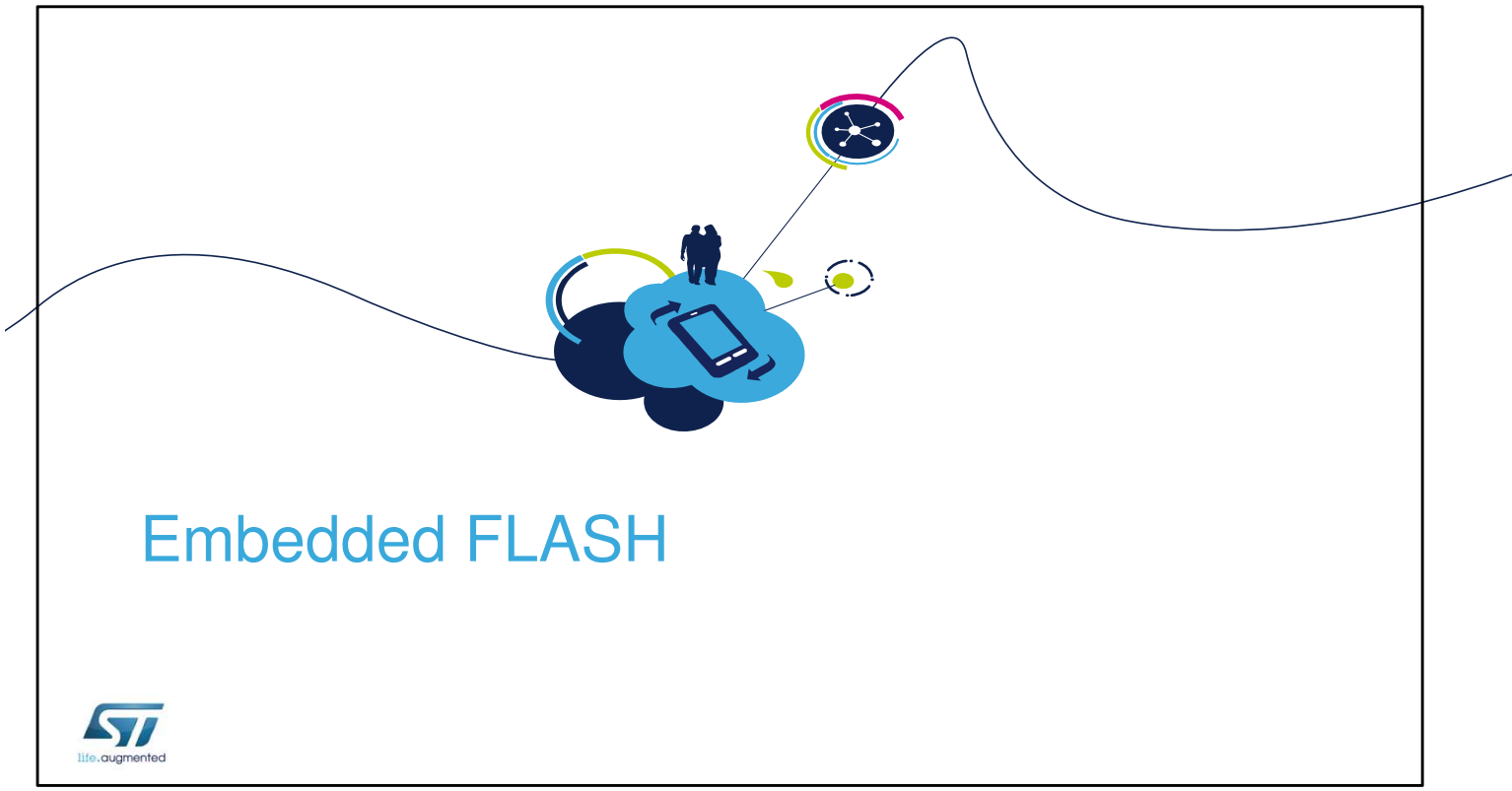
This slide presents the interrupt vector differences between STM32L4Rxxx/4Sxxx, STM32L4P5xx/4Q5xx and STM32L476xx/486xx devices.



Embedded FLASH

Let’s now go through the key new aspects of the flash memory between STM32L4+ Series and STM32L476xx/486xx devices.

STM32L4+ Flash Memory

- Up to 2 Mbytes : 256 pages
  - Single Bank: Page size = 8 Kbytes,
  - Dual Bank: Page size = 4 Kbytes
- 1 Kbyte OTP (one-time programmable)
- Flash memory read operations with two data width modes :
  - Single bank mode DBANK=0: read access of 128 bits
  - Dual bank mode DBANK=1: read access of 64 bits
- Protections:
  - Single Bank: 4 WPR areas, 2 PCROP areas
  - Dual Bank: 2 WPR areas per bank, 1 PCROP area per bank

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The flash memory can be configured by option byte (DBANK) in single bank mode with 128-bit read access or in dual bank mode with 64-bit read access.

Flash Memory Organization

DBANK Mode	Dual Bank (STM32L4 Series Compatible)				Single Bank			
Flash area	Flash memory addresses		Size (bytes)	Page#	Flash memory addresses		Size (bytes)	Page#
Main memory	Bank 1	0x0800 0000 – 0x0800 0FFF	4 K	Page 0	Single Bank	0x0800 0000 – 0x0800 1FFF	8 K	Page 0
		0x0800 1000 – 0x0800 1FFF	4 K	Page 1		0x0800 2000 – 0x0800 3FFF	8 K	Page 1
		-	-	-				-
		0x080F F000 – 0x080F FFFF	4 K	Page 255				
	Bank 2	0x0810 000 – 0x0810 0FFF	4 K	Page 0				
		0x0810 1000 – 0x010 1FFF	4 K	Page 1				
		-	-	-				
		0x081F F000 – 0x081F FFFF	4 K	Page 255		0x081F E000 – 0x081F FFFF	8 K	Page 255

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This slide presents the flash memory organization in single bank and in dual bank mode.

In dual bank mode, the main memory is divided into two 1-Mbyte banks, and each bank is split in 256 pages of 4 Kbytes.

In single bank mode, the main memory is a single 2-Mbyte bank split in 256 pages of 8 Kbytes.

Option Bytes New Features

	STM32L4+	STM32L476xx/486xx
Option bytes	nBOOT0	NA
	nSWBOOT0	NA
	DBANK (Dual bank mode)	NA
	DB1M (1MB/512KB dual-Bank)	DUALBANK (256/128 Dual-Bank)
	PCROP1_STRT[16:0] PCROP2_STRT[16:0]	PCROP1_STRT[15:0] PCROP2_STRT[15:0]
	PCROP1_END[16:0] PCROP2_END[16:0]	PCROP1_END[15:0] PCROP2_END[15:0]

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This slide presents the differences regarding the option bytes between STM32L4+ and STM32L476xx/486xx devices.

Flash Memory Wait States

STM32L4+ Series

CPU performance	Power performance	VCORE range	Typical value (V)	Max frequency (MHz)					
				0WS	1WS	2WS	3WS	4WS	5WS
High	Low	Range1: boost mode	1.28	20	40	60	80	100	120
		Range1: normal mode	1.2					NA	NA
Medium	High	Range 2	1.0	8	16	26	-	-	-

STM32L476xx/486xx

CPU performance	Power performance	VCORE range	Typical value (V)	Max frequency (MHz)					
				0WS	1WS	2WS	3WS	4WS	5WS
High	Low	Range1	1.2	16	32	48	64	80	-
Medium	High	Range 2	1.0	6	12	18	26		-

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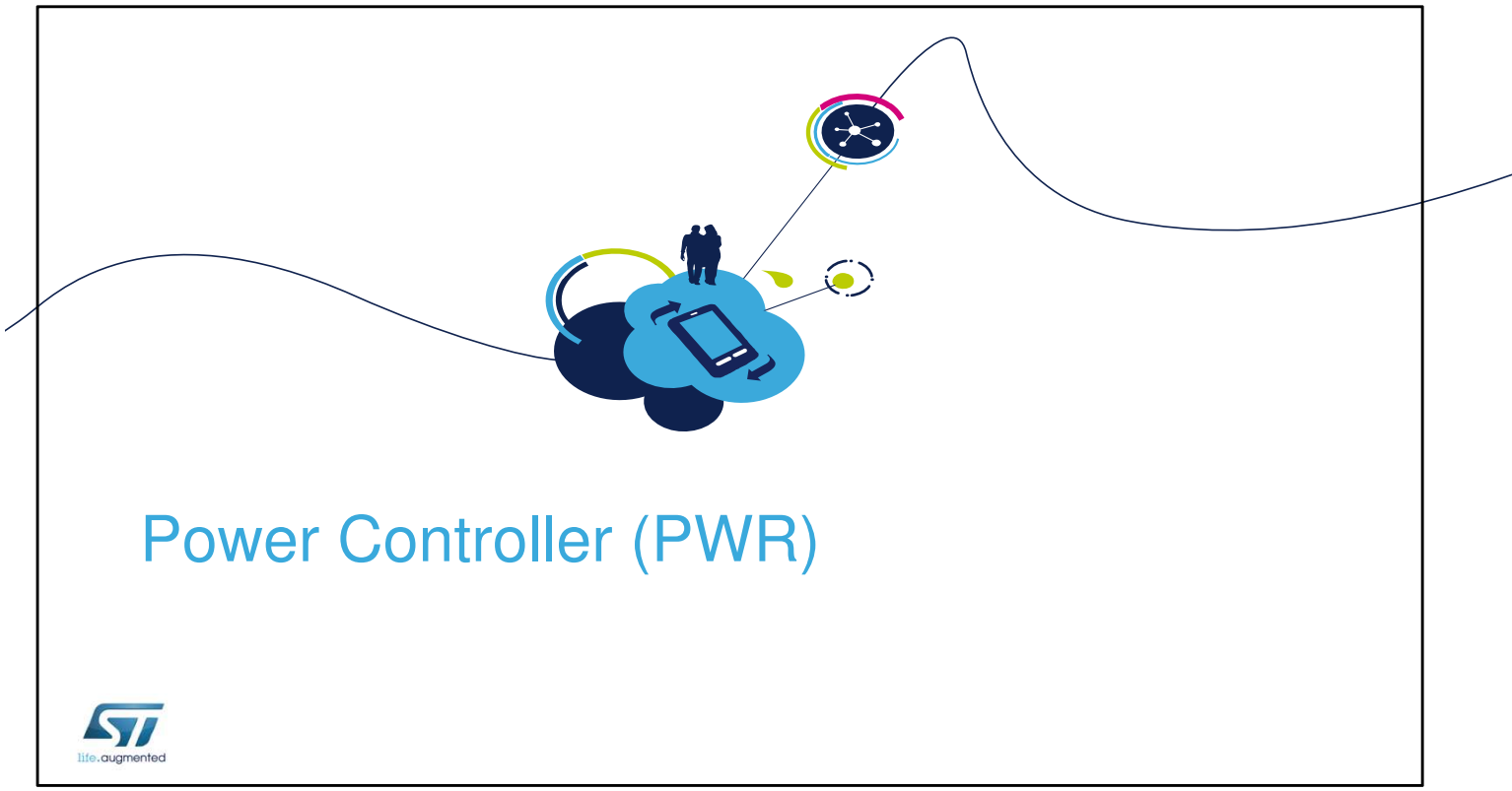
In order to read the Flash memory, it is necessary to configure the number of wait states to be inserted in a read access, depending on the clock frequency. The number of wait states also depends on the voltage scaling range.

The two tables present the differences in wait states between STM32L4+ Series devices and STM32L476xx/486xx devices.

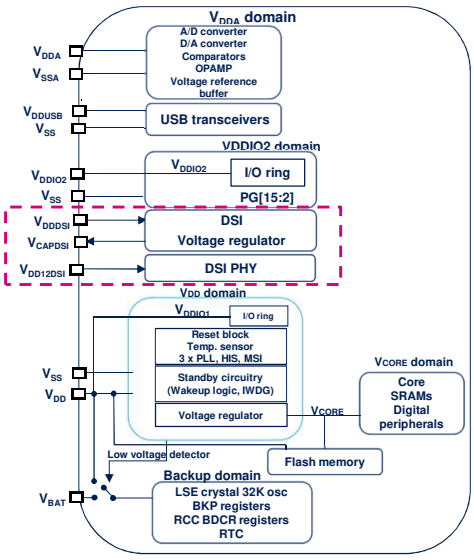


Power Controller (PWR)

More features are also added into the STM32L4+ microcontroller, which gives the user more flexibility.

Power Supply

- DSI power supply for STM32L4R9xx/S9xx
  - DSI (Display Serial Interface) power supply pins
    - VDDDSI an independent DSI power supply dedicated to the DSI regulator and MIPI DPHY
      - It must be connected to VDD
    - VCAPDSI the DSI regulator (1.2V) output
      - It must be connected to VDD12DSI.
    - VDD12DSI used to supply the MIPI D-PHY, clock and data lanes
      - A 2.2 µF must be connected to VDD12DSI
    - VSSDSI is an isolated ground supply used for DSI sub-system
  - If DSI is not used:
    - VDDDSI must be connected to VDD
    - VCAPDSI and VDD12DSI can be left floating
    - VSSDSI must be grounded

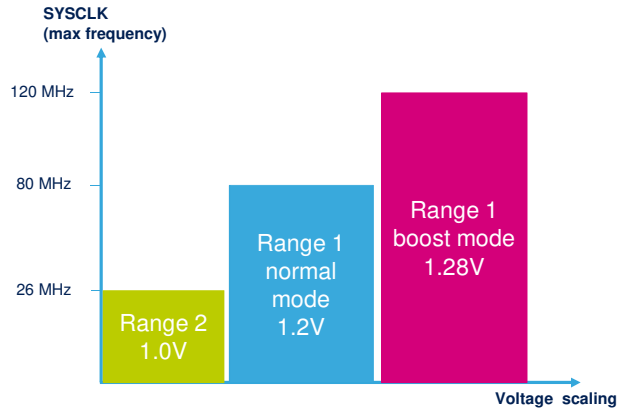


The STM32L4R9xx/S9xx devices feature the DSI (Display Serial Interface) sub-system and it uses several power supply pins which are independent from the other supply pins: VDDDSI, VCAPDSI and VDD12DSI.

If DSI peripheral is not used, the VDDDSI must be connected to VDD while VCAPDSI and VDD12DSI can be left floating.

Main Regulator: Voltage Scaling Range

- Main regulator output voltage:
  - Range 1 :
    - Boost mode: 1.28V
    - Normal mode: 1.2V (default after reset)
  - Range 2: 1.0V
- Power consumption optimization up to 10% in range1 normal mode vs boost mode



Caution: To use USB or DSI, range 1 boost mode **must be selected.**

The main regulator output voltage can be programmed by software in two power ranges Range 1 and Range 2.

In range1, the main regulator operates in two modes that can be selected by software :

- Range 1 normal mode: provides a typical output voltage at 1.2 V, allowing a system clock up to 80 MHz.
- Range 1 boost mode: provides a typical output voltage at 1.28 V, allowing a system clock up to 120 MHz.

The range 1 normal mode optimizes the power consumption up to 10% comparing to range 1 boost mode.

When you are using the USB or DSI peripheral, the range 1 boost mode must be selected.

Low Power Modes

	STM32L4+	STM32L476/486xx
Low Power Modes	STOP0	
	STOP1	
	STOP2 SRAM3 OFF	STOP2
	STOP2 SRAM3 ON	
	Standby SRAM2 (64 Kbytes) OFF(1)	Standby
	Standby SRAM2 (64 Kbytes) ON(1)	
	Shutdown	

(1) On STM32L4P5xx/4Q5xx devices SRAM2 can be fully (64 Kbytes) or partially (4 Kbytes) retained in Standby

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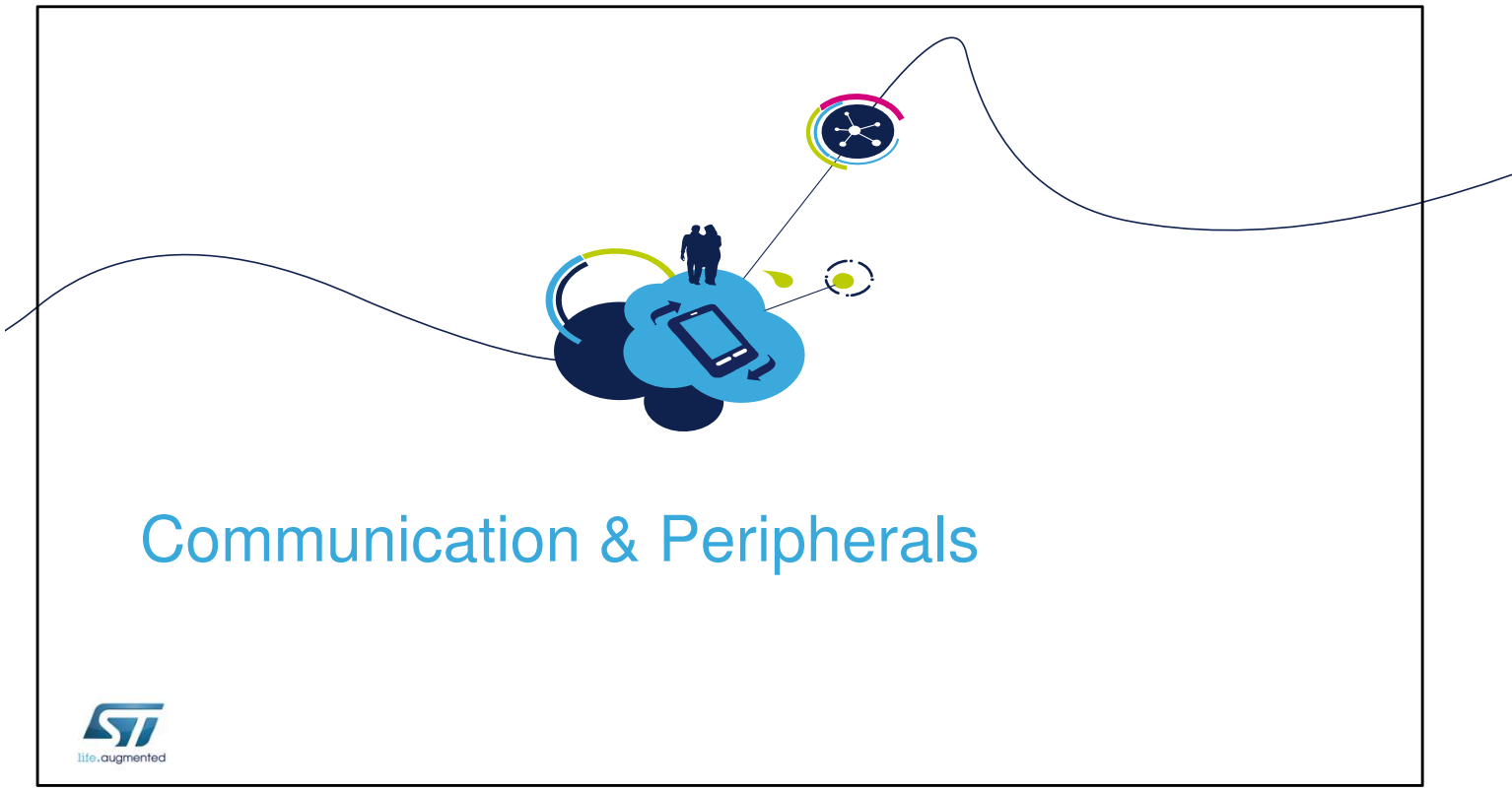
The STM32L4+ series features the same Low Power mode as the STM32L4 series with a new option to switch OFF or ON the SRAM3 during STOP2 mode and to switch OFF or ON the SRAM2 in Standby mode.

ULP Bench Score Differences

- The ULP Bench score is also impacted by the difference in consumption:

	L49x/4Ax	L47x/48x	L45x/46x	L43x/44x	L4Rxx/L4Sxx	L4P5xx/L4Q5xx
ULP Bench score	145	153	174.5	176.7	233	285

The ULP Bench score on STM32L4+ series devices is higher compared to the one on STM32L4 series devices.



Communication & Peripherals

The next tables detail the changes between the series concerning communications and peripherals.

STM32L476/486 Versus STM32L4+ Series

	STM32L4Rxxx/4Sxxx	STM32L4P5xx/4Q5xx	STM32L476/486
Power supply	1.71 ~ 3.6V with VBAT		1.71 ~ 3.6V with VBAT
Maximum Frequency	120MHz		80MHz
Flash	Up to 2MB	Up to 1MB	1MB
	Dual Bank (RWW) or Single Bank		Dual Bank (RWW)
System	SRAM1: 192KB	SRAM1: 128KB	SRAM1: 96KB
	SRAM2: 64KB		SRAM2: 32KB
	SRAM3: 384KB	SRAM3: 128KB	NA
	Backup-registers 32 x32-bit		
External Memory FSMC	8-,16-bit NOR, PSRAM, SRAM , FRAM and NAND memories • New data hold timing • New NBL setup timing • Clock divider =1		8-,16-bit NOR, PSRAM, SRAM and NAND memories
External Memory QuadSPI/OctoSPI	2x OctoSPI: Octal flash memories	2x OctoSPI: Octal flash + Octal PSRAM + HyperRAM memories Multiplexed mode	1x QuadSPI in single Flash mode
RCC	New clock source HSI48 for USB,RNG and SDMMC New PLLx divider, RTC APB clock gating		NA

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This table summarizes the key differences for system peripherals between the STM32L4+ series and STM32L476/786 devices.

STM32L476/486 Versus STM32L4+ Series

	STM32L4Rxxx/4Sxxx	STM32L4P5xx/4Q5xx	STM32L476/486
SYSCFG	ANASWVDD bit: GPIO analog switch control voltage selection : - VDDA or booster - VDD I2C4 Fast-mode Plus driving capability activation		NA
Peripheral Summary	PWR: New range 1 mode (Normal mode/ Boost mode) LP Mode: STOP2 + SRAM3 ON/OFF		PWR
	Standby + 64KB SRAM2 ON/OFF	- Standby + 64KB SRAM2 ON/OFF - Standby + 4KB SRAM2 ON/OFF	
	1x SDMMC Data transfer up to 104 Mbyte/s for the 8- bit mode.	2x SDMMC Data transfer up to 104 Mbyte/s for the 8- bit mode.	1x SDMMC Data transfer up to 50 MHz for the 8- bit mode.
	DFSDM (8x Channels, 4x Filters) (DFSDM audio, beamforming, internal ADC inputs, new trigger source)	DFSDM (4x Channels, 2x Filters) (DFSDM audio, beamforming, internal ADC inputs, new trigger source)	DFSDM (8x Channels, 4x Filters)
	OTG_FS with clock recovery		OTG_FS without clock recovery

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This slide continues the presentation of the key differences between STM32L476/786 devices and STM32L4+ Series devices – again the differences are highlighted in pink.

STM32L476/486 Versus STM32L4+ Series

	STM32L4Rxxx/4Sxxx	STM32L4P5xx/4Q5xx	STM32L476/486
Peripheral Summary	4 x I2C		3 x I2C
	-	PSSI	
	2x SAI (PDM mode on SAI1), new clock source (HSI)		2x SAI
	5x U(S)ART + 1x LPUART (FIFO, SPI slave transmission)		5x U(S)ART + 1x LPUART
	1xCAN		2xCAN
	1x ADC (12-bit)	2x ADC (12-bit)	3x ADC (12-bit)
	2x 12-bit DAC channels (updated triggers)		2x 12-bit DAC channels
	2xOPAMP, 2xCOMP		
	CRC/ 2x DMA / RTC / FIREWALL/ WWDG / IWDG / TIMx / LPTIMx /TSC/RNG		
	DMAMUX		-
	AES		-
	-	PKA	-
	HASH		-
	-		LCD
	-		SWPMI

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And here are some more peripheral updates between the two product lines.

STM32L476/486 Versus STM32L4+ Series

	STM32L4Rxxx/4Sxxx	STM32L4P5xx/4Q5xx	STM32L476/486
Graphic Peripherals	DMA2D with byte swap bytes tow by two (SB bit added) to support 18/24-bit mode (RGB888)		-
	MIPI-DSI Host (2 lanes)	-	-
	Chrom-GRC (GFXMMU)	-	-
	LCD-TFT		-
	Digital Camera interface (14-bit)		-

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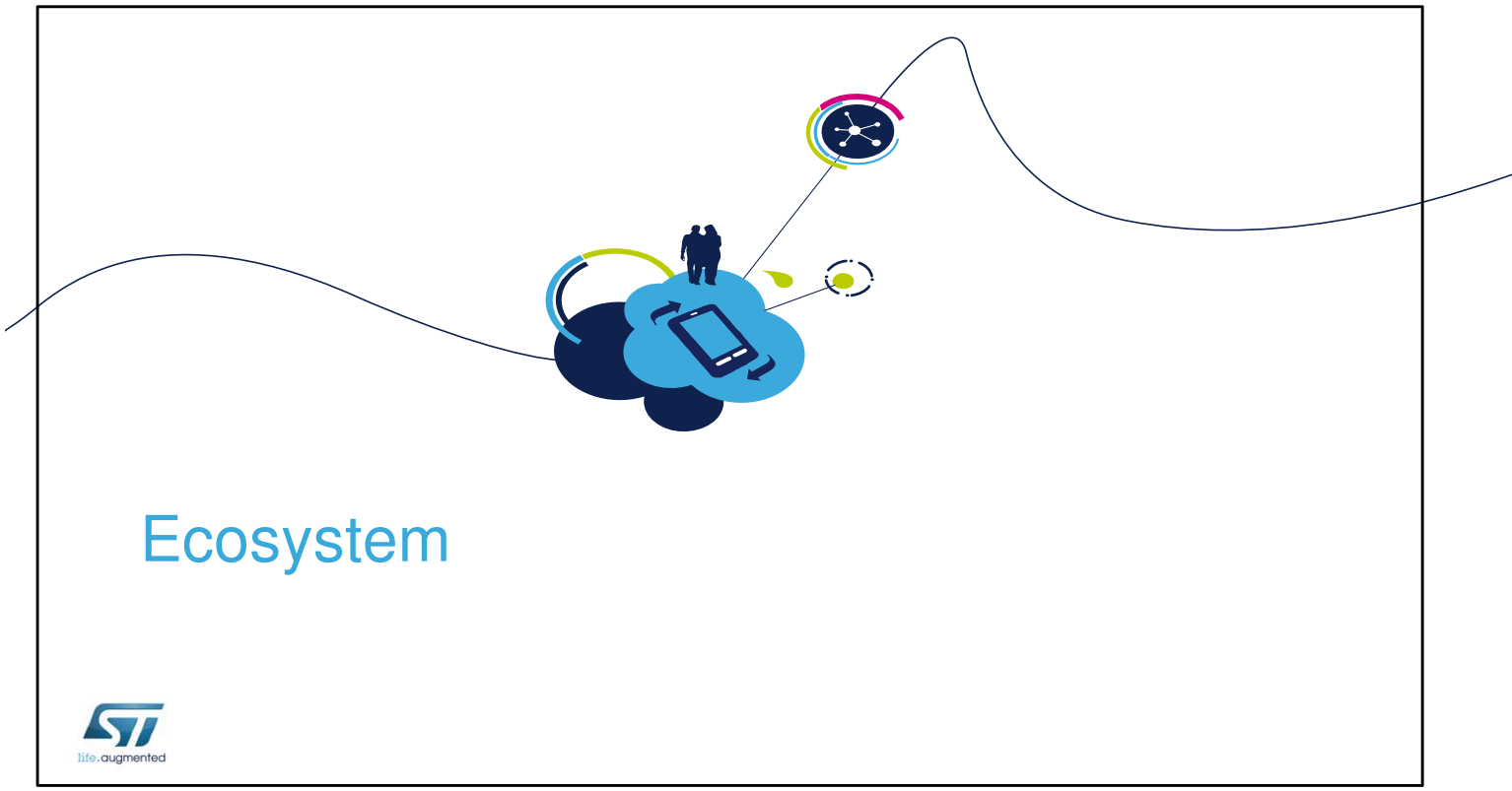
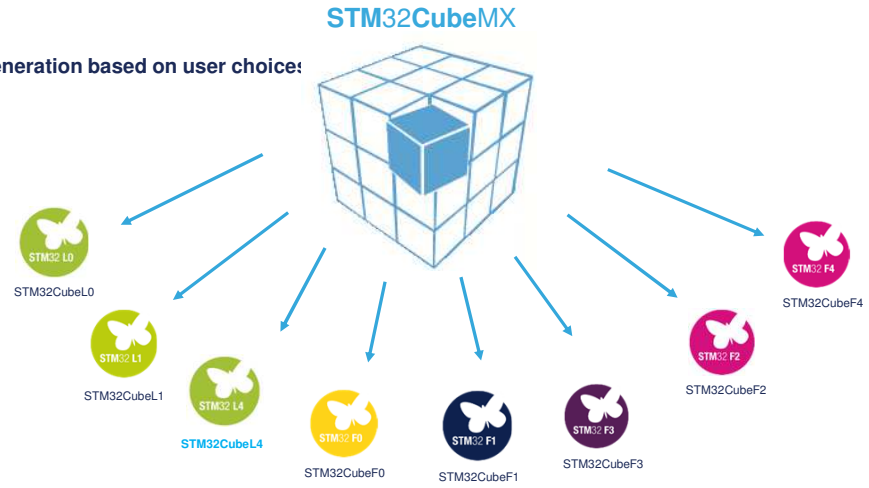
As already said in introduction, STM32L4+ embeds advanced graphic features enabling state-of-the-art Graphic User Interfaces.



And finally, even though the STM32L4+ series embeds many upgraded key features, the working environment remains the same!

STM32L4Plus Ecosystem

- Initialization Code generation based on user choices



STM32Cube HAL: Portable API within all series - Middleware stacks when applicable: RTOS, USB, TCP/IP, Graphics, …

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So the STM32L4 and STM32L4+ product family share the same software package known as the STM32Cube.
The STM32Cube HAL is a common library which addresses the entire STM32 microcontrollers family.
Specifically, the STM32L4 firmware package offers a standard HAL as well as Low Layer drivers and examples.
So if you are already using our STM32L4Cube, you just need to upgrade it from www.st.com to get the latest version.

References

- For more details, please refer to following sources
  - AN5017: Migrating between STM32L476xx/486xx and STM32L4+ Series microcontrollers

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For more details, please refer to application note AN5017 about the migration from STM32L476xx/486xx to STM32L4+ Series microcontrollers.