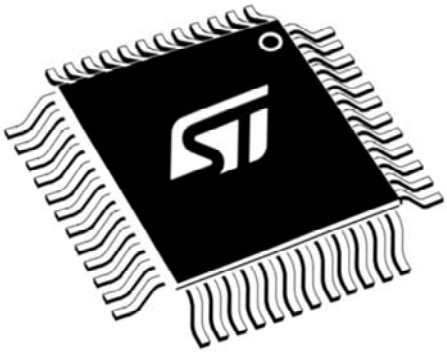
Hello, and welcome to this presentation of the STM32 general-purpose IO interface. It covers the general-purpose input and output interface and how it allows connectivity to the environment around the STM32F7 microcontroller.

Overview



- Provides interface for interaction with external environment
  - Fully configurable
  - With interrupt and wake-up capability
  - Direct connection to AHB bridge

Application benefits

- Direct microcontroller wake-up
- Supports a wide range of supply voltages
- Direct connection to AHB allows fast toggle response

life.augmented

The general-purpose IO pins of STM32 products provide an interface with the external environment. This configurable interface is used by the MCU as well as the other embedded peripherals to interface with both digital and analog signals. Application benefits include a wide range of supported IO supply voltages, as well as the ability to externally wake up the MCU from low-power modes.

Key features

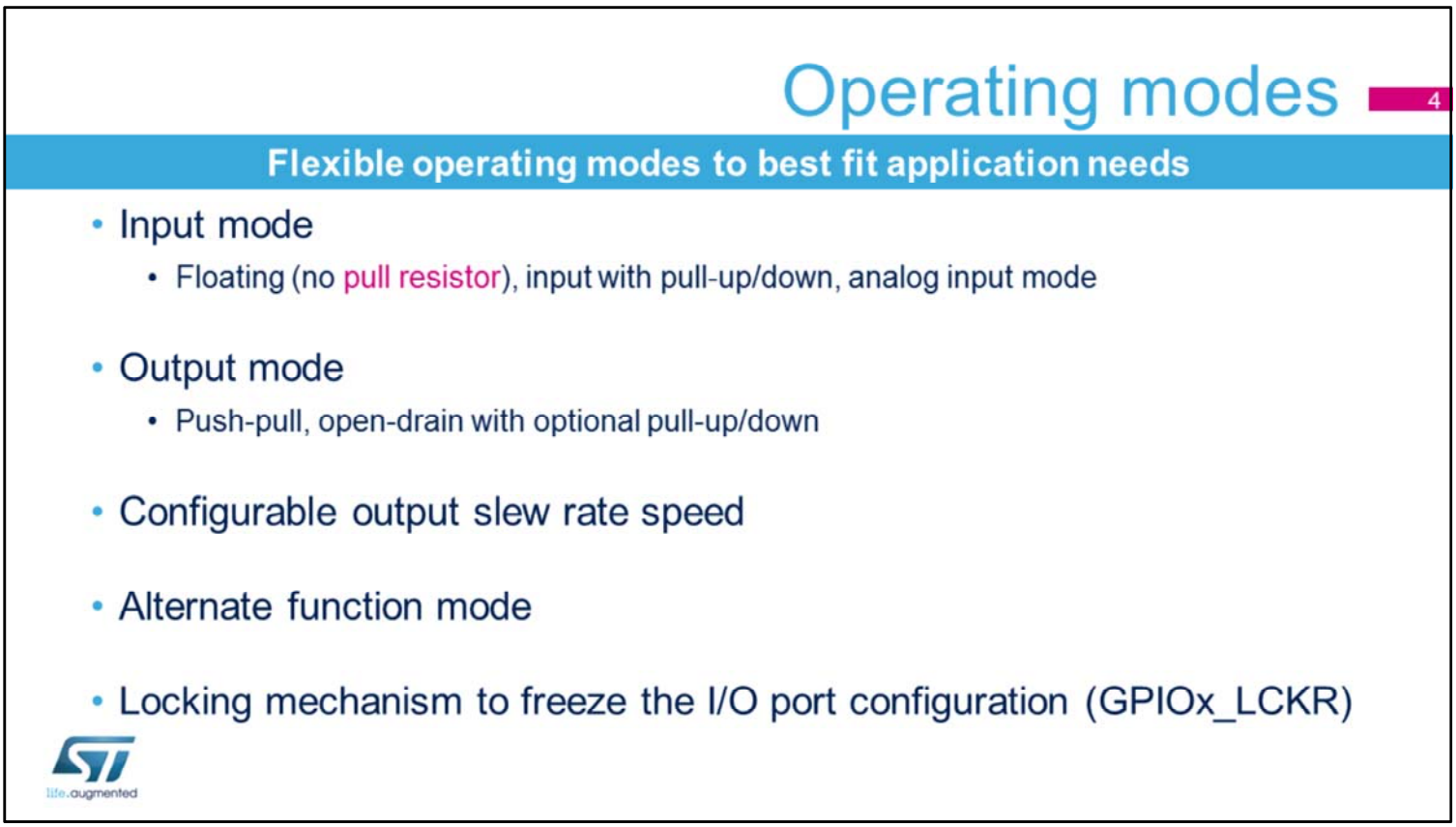
- Bi-directional operation of up to 168* I/O pins
  - Shared across 11 GPIOx ports named GPIOA to GPIOK, with up to 16 I/O pins per port
  - All with external interrupt and wake-up capabilities
  - Atomic bit set and bit reset operations using BSRR and BRR registers
  - Independent configuration for each I/O pin
- GPIOx directly connected to AHB bus
- Most I/O pins are 5 V tolerant when VDD is above 1.8 V

life.augmented

** : depends on part numbers and packages*

The general-purpose I/O ports provide bidirectional operation according to the input memory map.
I/O ports are directly connected to the AHB bus. This allows fast I/O pin operations, e.g. toggling and output, with an independent configuration for each I/O pin. They are shared across 11 ports named GPIOA to GPIOK, each of them hosting up to 16 I/O pins. I/O ports support atomic bit set and reset operations through the BSSRR and BRR registers. It allows I/O toggling every 2 clock cycles.
Most of the I/O pins are 5 V tolerant when supplied from VDD above 1.8 V.
Up to 10 I/O pins are supplied by independent voltage supplies (VDDUSB and VDDSDMMC). These supplies are independent of the VDD provided to the MCU.
This functionality allows users to adapt logic levels of the MCU's I/O pins to the levels required by external logic

which may be supplied by different voltage domains without the need for external level shifters.



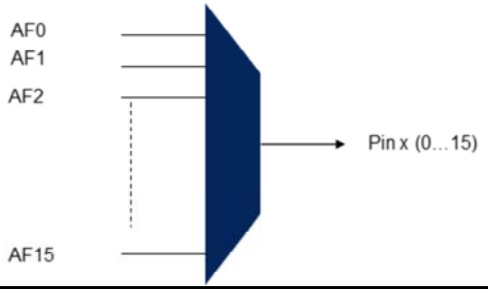
General-purpose I/O pins can be configured for use in several operating modes.
An I/O pin can be configured in an input mode with floating input, input mode with an internal pull-up or pull-down resistor or as an analog input.
An I/O pin could be also configured in an output mode with a push-pull output or an open-drain output with an internal pull-up or pull-down resistor.
For each I/O pin, the slew rate speed can be selected from 4 ranges to compromise between maximum speed and emissions from the I/O switching and adjust the application's EMI performance.
I/O pins are also used by other embedded peripherals to interface with the external environment. Alternate function registers are used to select the configuration for the peripherals in this case.
The configuration of the I/O ports can be locked to

increase robustness of the application. Once the configuration is locked by applying the correct write sequence to the lock register, the I/O pin’s configuration cannot be modified until the next reset.

Alternate functions

Structure of I/O pins is used as interface by other embedded peripherals

- Several embedded peripherals share the same I/O pins
  - Including USARTx_TX, TIMx_CHx, SPIx_MISO, EVENTOUT, …
- Alternate function multiplexer selects the peripheral connected to the I/O pin
  - Only one alternate function is connected to a specific I/O pin at a single time
  - Configurable through the GPIOx_AFRL and GPIOx_AFRH registers



Several integrated peripherals such as the USART, timers, SPI and others share the same I/O pins in order to interface with the external environment.
Peripherals are configured through an alternate function multiplexer which ensures that only one peripheral is connected to an I/O pin at a single time. Of course, this selection can be changed during run time of the application through the GPIOx_AFRL and AFRH registers.

Special considerations for I/O pins

Only debug pins remain in AF mode under reset

- During and after reset, the alternate functions are not active
  - I/O ports default state to input mode
  - To save current consumption IOs might be configured to analog mode
- Only JTAG/SWD debug pins remain in AF pull-up/pull-down configuration
  - PA13: JTMS/SWDIO
  - PA14: JTCK/SWCLK
  - PA15: JTDI
  - PB3: JTDO
  - PB4: NJTRST

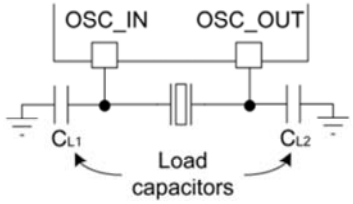
life.augmented

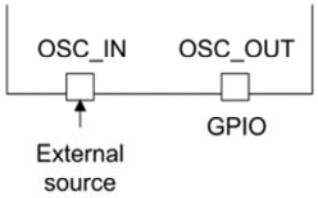
During and after reset, the alternate functions are not active.
Only debug pins remain in AF mode.
JTAG/SWD debug pins remaining in AF configuration mode are listed in this slide.

Special considerations for HSE/LSE pins

Oscillator pins can be used as standard I/O pins

- When the oscillator is switched OFF, related pins behave as I/O pins
  - Valid for both HSE / LSE
  - This state is the default one after reset
- When user external clock mode is used, the second pin behaves as an I/O pin
  - Only OSC_IN or OSC32_IN is used as clock source
  - OSC_OUT and OSC32_OUT are standard I/O pins





When the external oscillator is switched off, pins related to this oscillator can be used as standard I/O pins. This is the default state after device reset.
When the external clock source is used instead of a crystal oscillator, only related OSC_IN pin is used for the clock and OSC_OUT pin can be used as standard I/O pin.