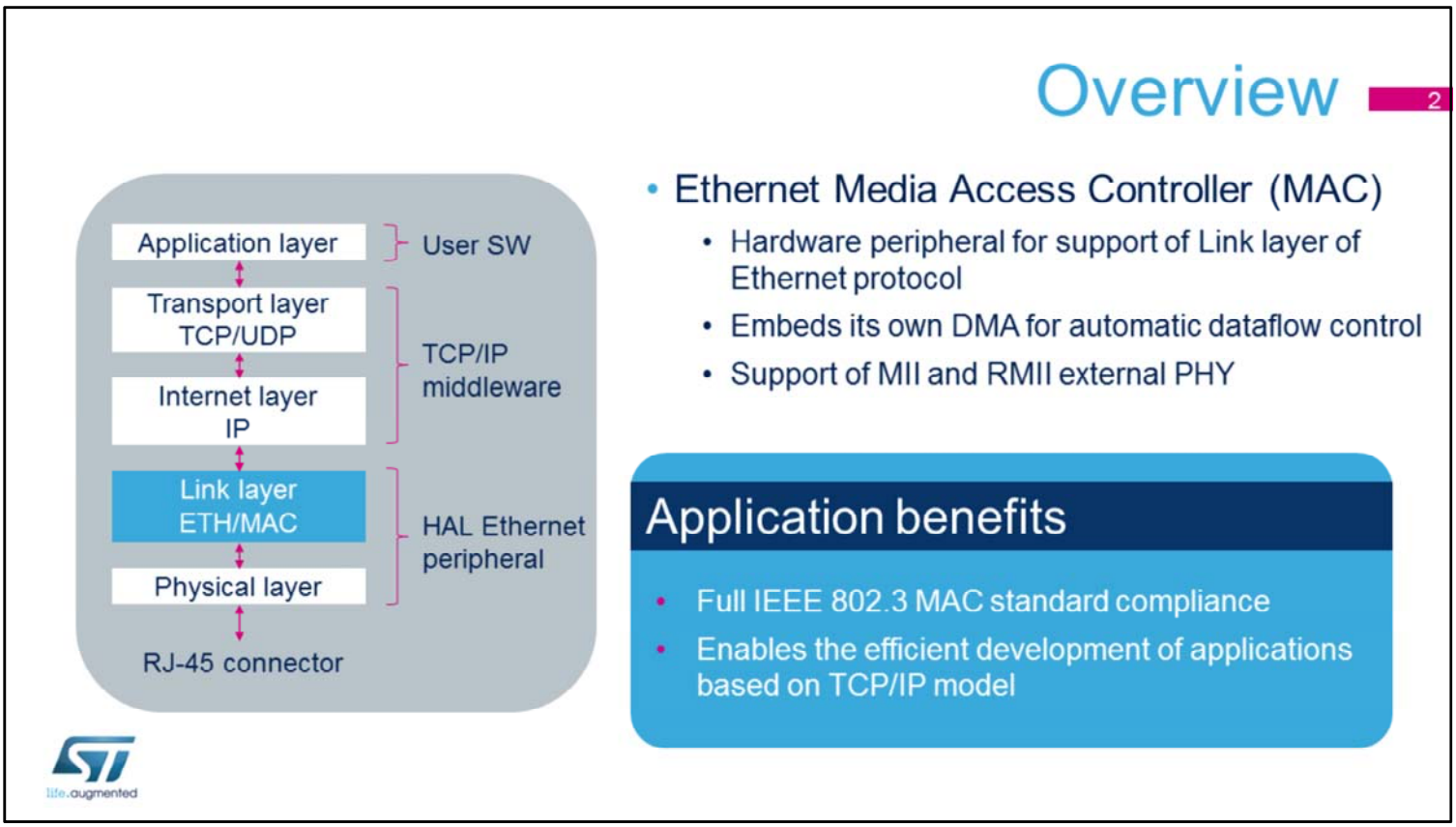
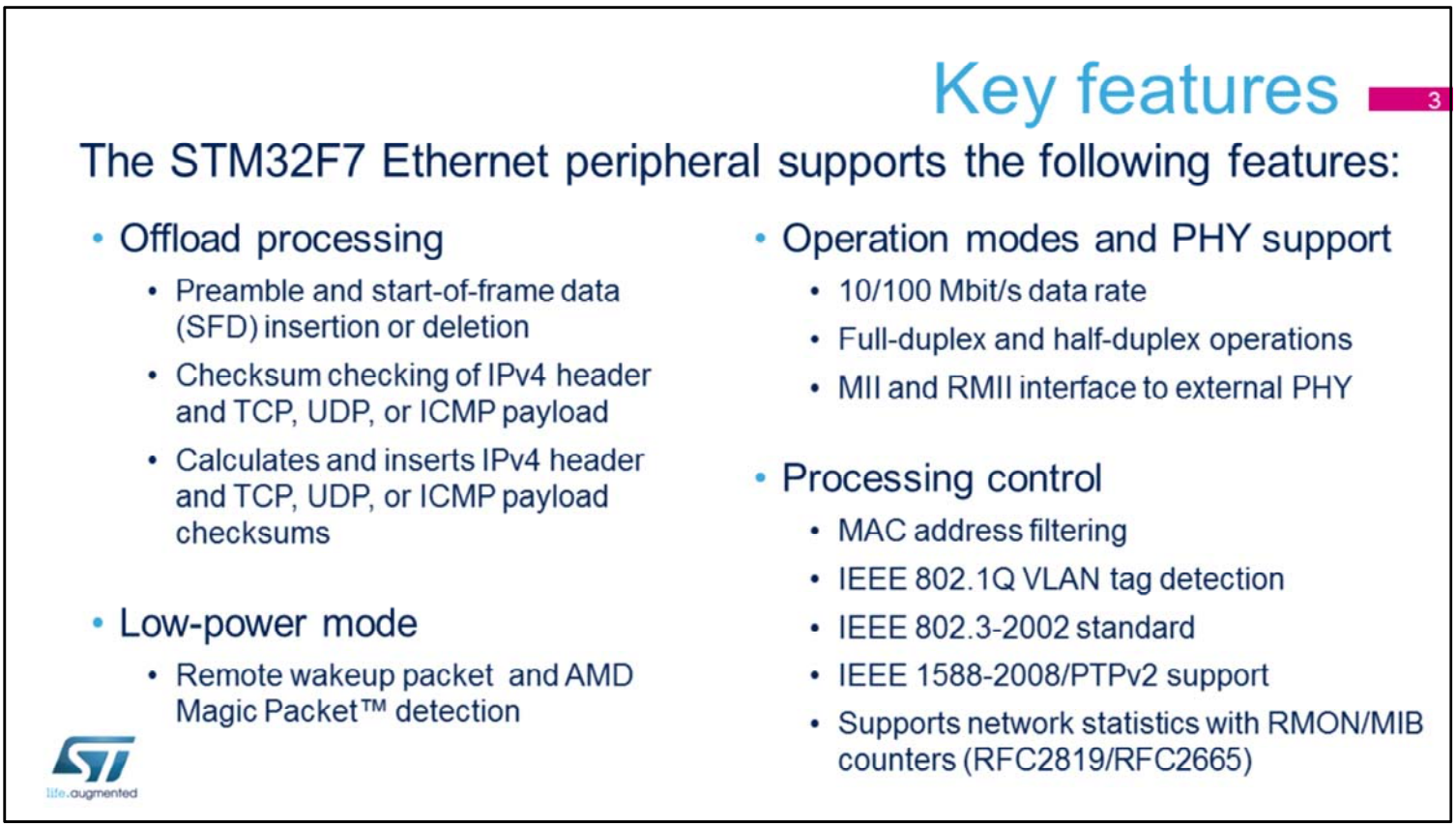
Hello, and welcome to this presentation of the STM32F7's Ethernet MAC peripheral
This peripheral is in charge of the Media Access Control layer of Ethernet communication.



The peripheral presented in these slides is a Media Access Controller, or MAC, for Ethernet protocol. It is fully compliant with the IEEE 802.3 standard.

The peripheral is involved in applications based on internet networks. Such applications rely on the TCP/IP layer model as presented in the diagram.
The MAC is in charge of the link layer of TCP/IP communication model.
Upper layers are managed by software. For example, Transport and Internet layers can be managed by the popular LwIP stack.
Finally, the physical layer, or PHY, is supported by external components and linked to an RJ45 connector.



The key features of the STM32F7 Ethernet MAC peripheral are presented in this slide.

The peripheral supports both full- and half-duplex modes of operation at either 10 or 100 Mbps . Auto-negotiation between the peripheral and the external PHY enables automatic configuration of the operation mode. The external PHY is supported through two interface types: The typical Media-Independent Interface, or MII, and the Reduced-MII that needs twice less pins than MII.

Among the advanced features supported by the peripheral, we can list:
- Frame filtering based on MAC address or VLAN tags,
- Precision Timing Protocol support with high precision time-stamping of frames,
- Several network statistics registers available to monitor the connection quality.

In addition to the previous features, the peripheral brings several types of heavy processing offloading. It supports automatic management of preamble and start-of-frame tags, checksum checking for received frames and checksums computation and insertion for transmitted frames.

A functional low power mode reduces power consumption by stopping the peripheral until special packets are received. This enables a network-controlled system wakeup.

Offload features

Ethernet datagram management overview

- Ethernet datagram offload processing

1. Preamble and Start-of-Frame tag automatic insertion (Rx) or deletion (Tx)
2. Destination MAC address filtering
3. Source MAC address filtering
4. VLAN tag detection of received frame
5. Checks frame type and size (Rx) or Insert field (Tx)
6. Ethernet payload Checksum computation and insertion (Tx) or checking (Rx) for:
   - IPv4 header
   - TCP/UDP/ICMP payload
7. Datagram CRC computation (Tx) and checking (Rx)

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This slide presents the offload processing managed by the peripheral on an Ethernet datagram.
You can see that most of the non-payload part of the datagram is efficiently managed in hardware.

The preamble and SFD are basic synchronization patterns and are inserted or deleted automatically.

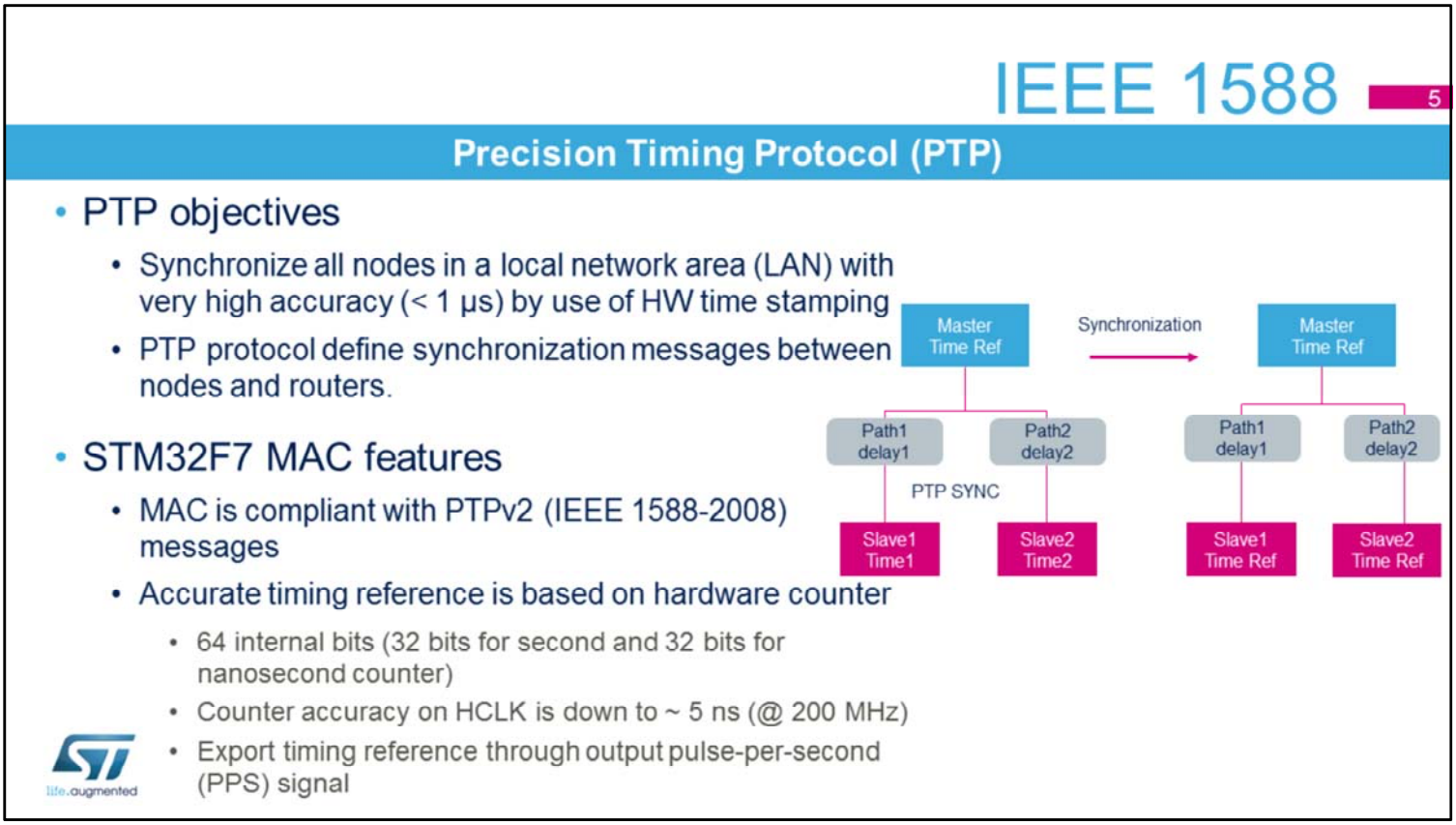
MAC address filtering is recommended to select only the frames that are relevant for your application. The MAC supports multiple filtering options for unicast or multicast address frames and perfect or hash filtering.

VLAN-tagged frames are supported. Received frames are signaled to the host after VLAN tag comparison.

Payload is composed of data from transport or internet layers. The checksum is computed or checked for IPv4

headers and TCP/UDP of ICMP payload.

Finally, the CRC is computed for the whole datagram without taking into account the preamble and the start-of-frame tag.



The precision timing protocol has been developed to support high precision synchronization between several nodes of an Ethernet network. The targeted precision is approximately 1 us.
This level of precision can only be achieved by hardware support for packet time-stamping.

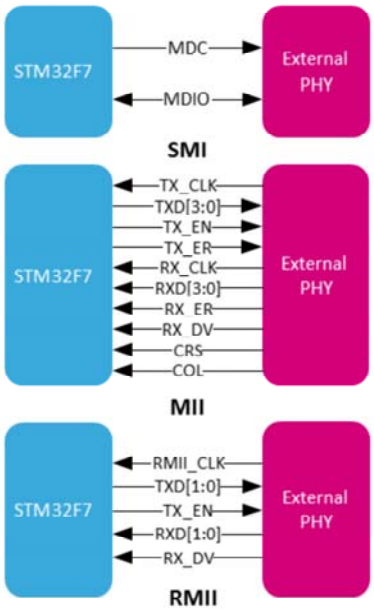
STM32F7 supports PTP messages for synchronization and acknowledge.
A 64-bit register indicates the current value of the system time maintained by the MAC.

A pulse-per-second signal (or PPS) can be driven on the Timer 2 so that the timing drift between slave and master clock can be measured.

PHY interface

Media-Independent Interfaces (MII)

- PHY control interface
  - Station Management Interface (SMI)
    - Two-wire MDIO Interface to PHY
    - Enables control of PHY register
    - Compliant with IEEE 802.3 Clause 22
- PHY data interfaces
  - Media Independent Interface (MII)
    - 16-signal interface
  - Reduced MII (RMII)
    - 7-signal interface

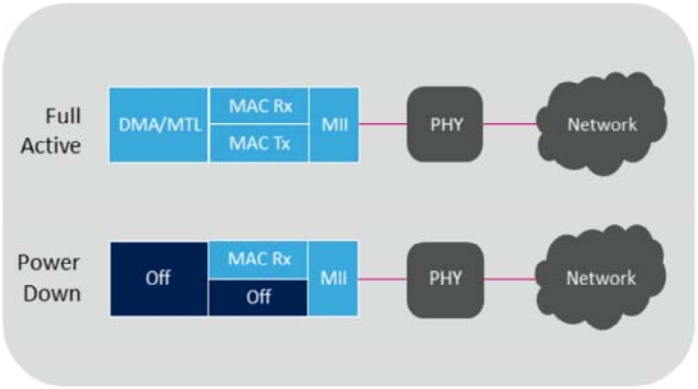


The external PHY is controlled by the peripheral through the Station Management Interface (SMI) that allows read and write access to PHY internal registers. This interface supports the MDIO protocol on a pair of wires. Read and Write operation codes are available.

Two types of interfaces are supported by the peripheral; both supporting full- and half-duplex operations at 10 or 100 Mbit/s
These interfaces are the classical Media-Independent Interface, or MII, that requires 16 signals between both devices, and the Reduced-MII that requires only 7 signals and then allows IO saving.

Power management

Remote wakeup frame detection



- Power-down mode state
  - Application and Tx clock are switched-off
  - PHY, MII interface and MAC Rx remain active
  - All packets but wake-up ones are dropped
- Wake-up
  - Wake-up is controlled by the network
  - Wake-up packets are
    - AMD Magic packet
    - User defined
  - Wakeup frame detection is an event that can wakeup the system from Stop mode

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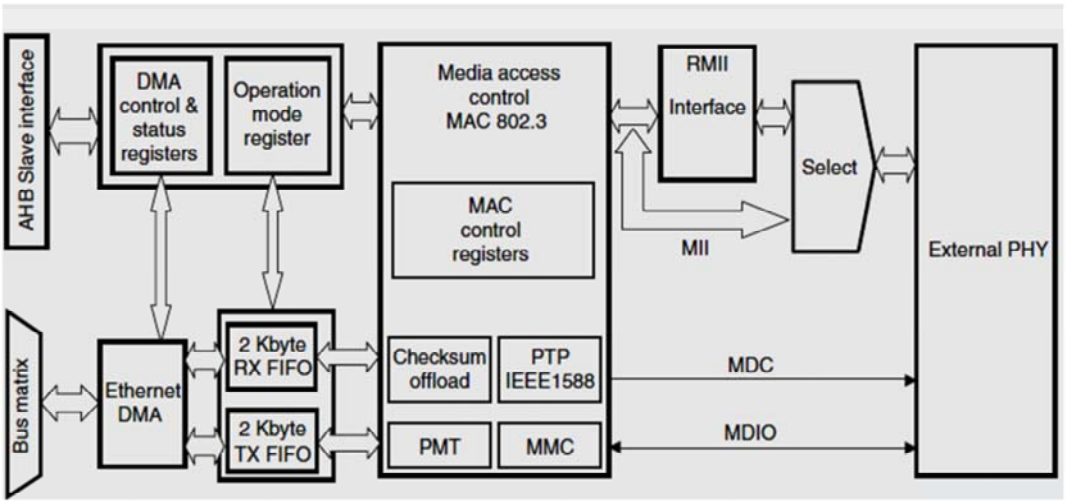
A functional low power mode enables power consumption saving by stopping the DMA and Transmit path clocks. The Receive path of the peripheral remains active in order to detect of special wakeup packets.
This feature enables a system wakeup from Sleep or Stop mode controlled by network.

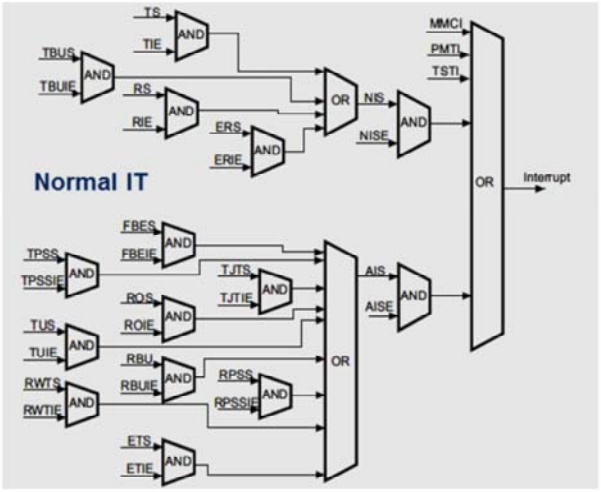
Block diagram



This slide presents the peripheral block diagram.

The Ethernet peripheral embeds
- Its own DMA for autonomous direct memory interface
- Internal FIFOs for Rx and Tx queues for dataflow management
- A media access controller (MAC) supporting most functional features detailed in previous slides: Offload engines, Precision Timing Protocol, Power Management (PMT) and MAC management counters for statistics gathering
- A PHY interface block supporting Media Independent Interface (MII) and Reduced MII

Interrupts



- Ethernet MAC Interrupts are split into three categories
  - DMA Normal Interrupts
    - Good transmission or reception
  - DMA Abnormal Interrupts
    - Rx FIFOs overflow
    - Tx FIFO underflow
    - Process stopped
  - MAC Interrupts
    - PMT: Set when a wakeup packet is received
    - MMC: Set when there is a MMC counter event
    - TST: Set when target time is reached
- All interrupts can be masked

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The Ethernet MAC peripheral supports various interrupts. All these interrupt lines can be masked and converge to the same output signal as you can see on the diagram.

For transmission and reception interrupts, a distinction is done between normal and abnormal operations. Abnormal operations refer to process aborted or FIFOs in overflow or underflow state.

Special MAC features have their own interrupts:
- In low-power mode, wakeup packet reception is signaled on the PMT line.
- Any update of MMC counters can trig an interrupt too.
- And finally an interrupt line is dedicated to the Precision Timing Protocol.

Low-power modes

Mode	Description
Run	Active.
Sleep	Active. Peripheral interrupts cause the device to exit Sleep mode.
Stop	The Ethernet peripheral is able to detect frames while the system is in Stop mode, provided that EXTI line 19 is enabled.
Standby	Powered-down. The peripheral must be reinitialized after exiting Standby mode.

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Here is an overview of the peripheral's status in each of the low-power modes.
Only PMT mode is available in Stop mode. In this mode, the peripheral waits for wakeup packets.

References

- Ethernet peripheral is compliant with the following standards:
  - IEEE 802.3-2002 for Ethernet MAC, MII
  - IEEE 1588-2002 and IEEE 1588-2008 for Precision Timing Protocol (PTP)
  - IEEE 802.1Q-2005 for Virtual Bridged Local Area Networks (VLAN)
  - RMII specification from the RMII consortium
- For more details, please refer to:
  - UM1713: Developing applications on STM32Cube with LwIP TCP/IP stack (User manual)

The Ethernet is compliant with the following standards:
• IEEE 802.3-2002 for Ethernet MAC
• IEEE 1588-2008 standard for precision networked clock synchronization
• RMII specification from the RMII consortium