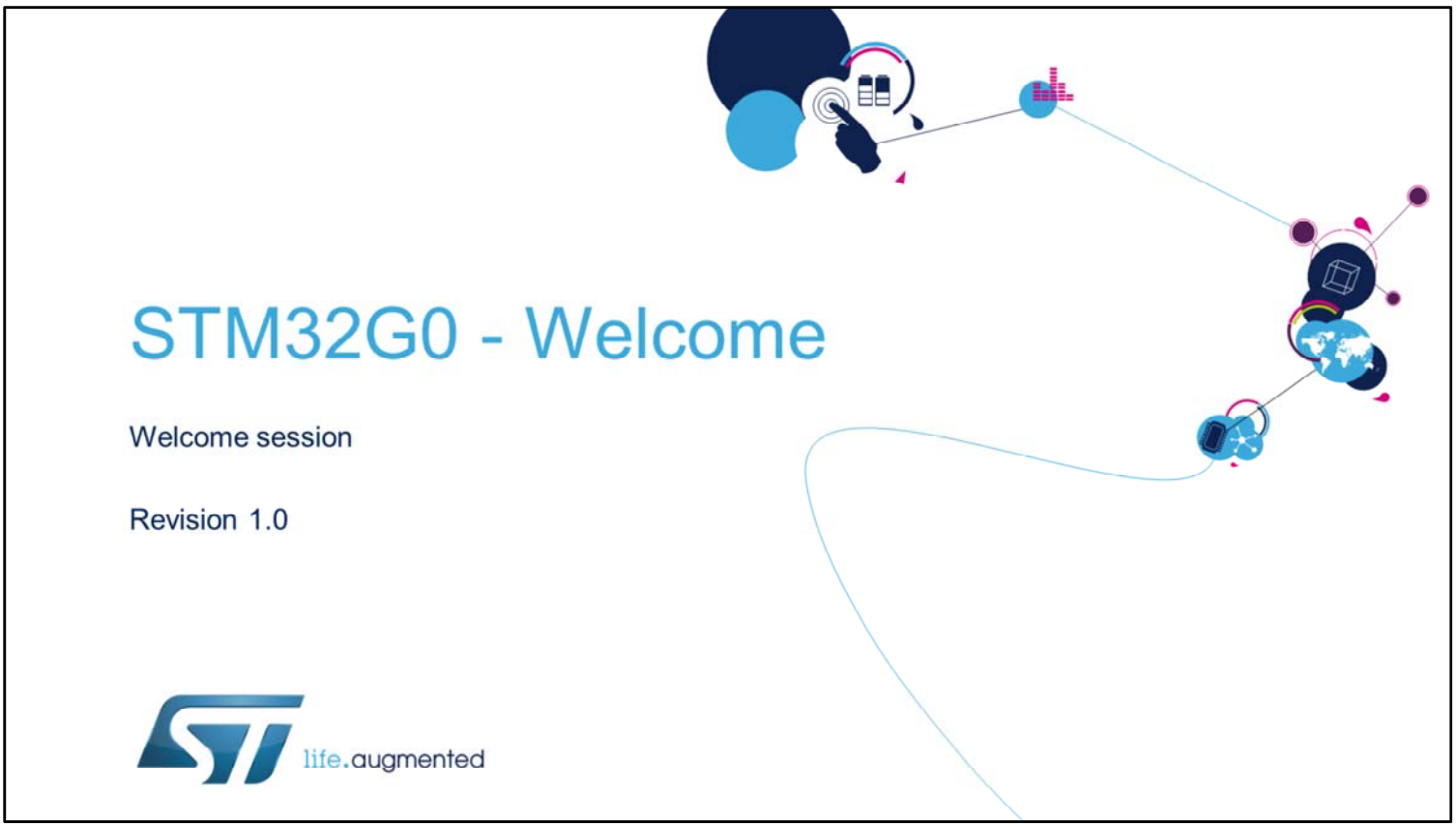
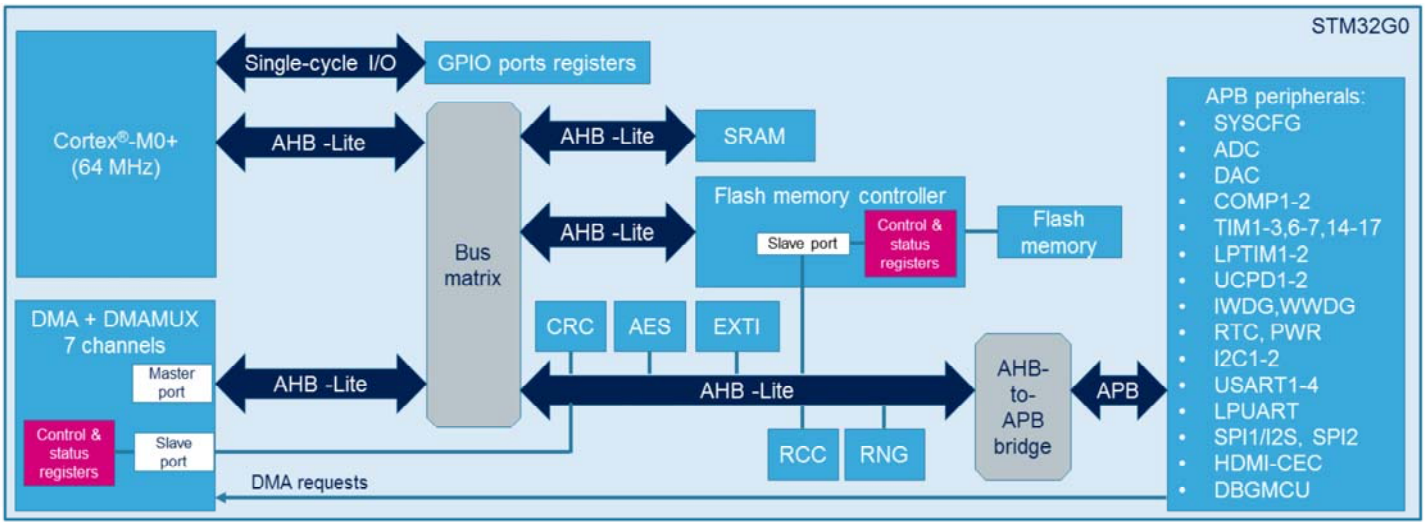


Hello, and welcome to the STM32G0 training session.

STM32G0 Architecture



The architecture of the STM32G0 is described in this figure.
The STM32G0 is a low-power microcontroller whose CPU is an ARM Cortex-M0+.
Only the GPIO ports are directly accessible from the CPU by using the single-cycle I/O bus.
Two masters are connected to the main AHB interconnect, called bus matrix in the figure, the CPU and also the DMA controller.
The AHB slaves are:

- Memories: SRAM and Flash memory
- CRC, AES, RCC, RNG, EXTI peripherals
- Flash controller registers
- DMA-DMAMUX registers
- The AHB-to-APB bridge.

The APB peripherals are listed in the blue box on the

right of the figure.
Most peripherals can request a DMA transfer to the DMAMUX and then the DMA Controller in order to transfer data to/from SRAM or Flash memory.
For instance, characters received by USART1 can be transferred to a buffer in SRAM without software intervention, by relying on a DMA channel.

STM32G0 Ordering Information

Example: STM32 G 081 R B T 6

Device family	STM32	Arm® based 32-bit microcontroller
Product type	G	General Purpose
Device subfamily	070	Value line
	071	Access line
	081	Security line
Pin count	E	25
	G	28
	K	32
	C	48
	R	64
Flash memory size	8	64 KB
	B	128 KB
Package type	I	UFBGA
	T	LQFP
	U	UFQFPN
	Y	WLCSP
Temperature range	6	-40 to 85°C (105°C junction)
	3	-40 to 125 °C (130 °C junction)
Options	xyy	xTR = tape and reel packing; x = N (PD product version) or blank x$_{__}$ = tray packing; x = N (PD product version) or blank other = 3-character ID incl. custom Flash code and packing information; x = N for PD product version

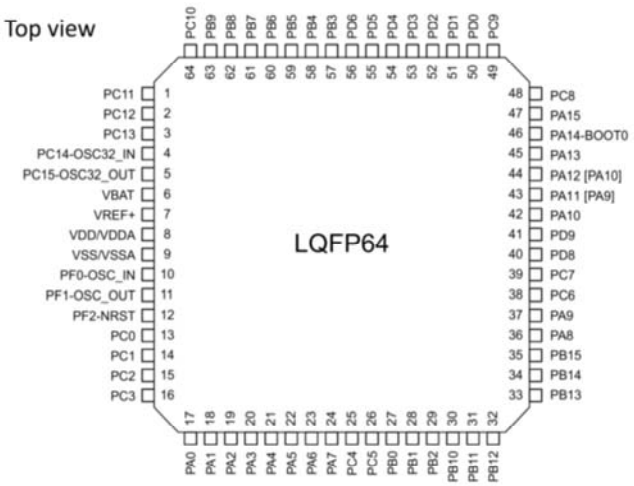
life.augmented

This slide explains the various fields of the STM32G0 ordering information.
Device family is STM32, Product Type is G, Device subfamily can be 070 for Value line, 071 for Access line and 081 for Security line.
Four pin counts are supported: from 25 to 64 pins, with respectively 23 to 60 GPIOs.
The Flash memory size can be 64 or 128 Kbytes.
The following packages are proposed: UFPGA, LQFP, UFQFPN and WLCSP.
Two temperature ranges are supported: -40 to 85°C and -40 to 125 °C
The last field indicates the options: typically blank or N depending on whether USB Power Delivery interface number 2 pins are available in 28- and 32-pin packages.
Therefore, the STM32G081RBT6 is a STM32G0, Security line, 64-pin, 128-Kbyte Flash memory, LQFP

MCU, supporting -40 to 85°C temperature range.

STM32G0 Packages

- STM32G0 features one power supply V_{DD}/V_{DDA}
- V_{BAT} and V_{REF+}:
  - Not present in small packages
- All other system pins can be replaced by GPIOs:
  - NRST multiplexed with PF2
  - BOOT0 multiplexed with PA14



Most of the pins are GPIOs supporting multiple functions. Dedicated pins are power supply and ground. Power supply pins are VDD, VBAT and VREF+.
Note that VBAT and VREF+ pins are not present in 32-, 28-, and 25-pin packages.
The reset signal is multiplexed with GPIO Port F number 2 and BOOT0 is multiplexed with GPIO Port A number 14. So these IO pads have a dedicated function during reset time and become later general-purpose I/Os.

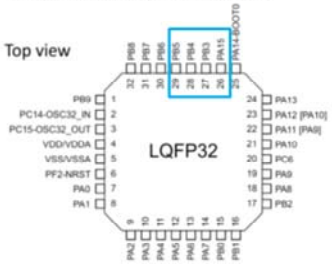
STM32G0 USB Power Delivery

- The following table indicates the number of USB Power Delivery units present in the package according to the pin count:

Pin count	USB PD support	
64	UCPD1 and UCPD2	
48	UCPD1 and UCPD2	
32	GP	UCPD1
	PD	UCPD1 and UCPD2
28	GP	UCPD1
	PD	UCPD1 and UCPD2
25	PD not supported	

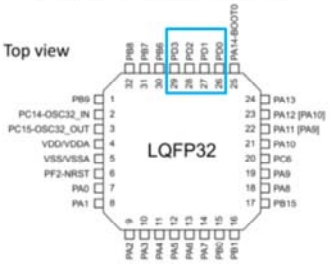
- GP Version: STM32G071KxT
  - General-purpose pinout

Top view



- PD Version: STM32G071KxTxN
  - Power Delivery pinout

Top view



Pin	Additional functions
PD0	UCPD2_CC1
PD1	UCPD2_DBCC1
PD2	UCPD2_CC2
PD3	UCPD2_DBCC2

life.augmented

The devices housed in 64- and 48-pin packages provide two USB-C Power Delivery ports.
The devices housed in 28/32-pin packages come in two variants – GP with a single-port limited USB-C Power Delivery and PD with 2-port USB-C Power Delivery.
This slide highlights the differences between the packages supporting and not supporting 2-port USB-C Power Delivery (PD2).
On the left, the STM32G071KxT supports a unique Power Delivery interface: PD1.
On the right, the STM32G071KxTxN supports two Power Delivery interfaces PD1 and PD2.

The STM32G0 has three power supply pins: VDD/VDDA, VBAT and VREF+.
VDD/VDDA is the power supply of the IO pads and integrated Flash memory and also supplies voltage regulators which provide the Vcore supply. The Vcore voltage is 1.2V for a system clock frequency of 64 MHz.
The VBAT power domain, consuming very little energy, includes RTC, and LSE oscillator, tamper detection and backup registers.
The VREF+ is the input reference voltage for ADCs and DACs. It is also the output of the internal voltage reference buffer when enabled.
On packages where VREF+ and VBAT are not available, these power supplies are internally connected to the VDD pin.
The STM32G0 offers a new security feature called Securable Memory Area. The main purpose of the

securable memory area is to protect a specific part of Flash memory against undesired access. This allows implementing software security services such as secure key storage or safe boot.
The general-purpose Input/Outputs (GPIOs) can sink or source up to ±8 mA, and sink or source up to ±20 mA.
The STM32G0 supports FlexPowerControl which enables: efficient running, seven low-power modes, and several sub-modes.
In Run mode, the consumption is 100 microamperes per megahertz.
Stop 0 and Stop 1 are low-power modes in which the state of the Cortex-M0+ is maintained. Stop 1 is equivalent to Stop 0 with main regulator off, resulting in a smaller current consumption but longer wake-up time.
In Stand-by mode, by default: there is neither SRAM nor registers retention, because voltage regulators are in power-down state. However there is an option to retain the contents of the entire SRAM.
Shutdown mode is similar to Standby but without power monitoring and the unique clock source is the low-speed external oscillator.

The STM32G0 integrates the following subsystems:

- System modules: PWR, RCC, RTC and Tampers, Systick, GPIO, CRC and SYSCFG
- Processor modules: Cortex-M0+ core, MPU, NVIC, and SW debug
- DMA controller, supporting 7 channels
- Interconnect, based on an AHB-Lite matrix and an AHB-to-APB bridge
- Embedded memories: 128-Kbyte Flash memory + 36-Kbyte SRAM
- Control modules: one 32-bit timer, one 16-bit timer that can be used to control a motor, five 16-bit timers with PWM capability, two low power timers
- Analog modules: temperature sensor, 12-bit ADC, 12-bit DAC, and two comparators
- USB Power Delivery modules: 2 modules including BMC and PHY

- Connectivity modules: two SPI modules also supporting I2S, four USARTs, one LPUART, two I2C controllers, one HDMI CEC
- Encryption modules: AES and true RNG.

This session is organized to provide you with the most important information to ensure that you can develop your application as easily as possible. You will find a technical description of all the STM32G0 modules including peripherals and development tools organized into specific sections: system, ARM Cortex®-M0+ CPU, interconnect and DMA controller, memories, control, analog, USB Power Delivery, connectivity, encryption and development ecosystem.

You can browse each section separately and learn about each module in the order of your choice and at your convenience.

This session also allows you to search directly for a keyword and you will have a direct access to the sections covering this information.

Now let’s get started with the training. Do not hesitate to follow the events and news about this product on our website at www.st.com/stm32g0.
Enjoy!