AN2441
Application note

Low cost effective oscillator for STR71x MCUs

Introduction

The STR71x 32-bit MCU family from STMicroelectronics runs with an external oscillator which is connected to the CK pin.

A straightforward solution for the external oscillator is to purchase an oscillator chip which fits the application requirements. However, this solution is normally costly. This application note gives the user a low cost oscillator solution with discrete components and based on a resonator or quartz.

Resonators have shorter start-up time compared to crystals but they have less frequency accuracy. Depending on the application requirements, users can choose between short start-up time and frequency accuracy. In this application note, a quartz crystal is used in the oscillator circuitry.

There are two primary quartz-controlled oscillators circuitries. Such circuitries are generally described by the type of crystal unit used:

- Series resonant oscillator (when a series resonant quartz crystal is used)
- parallel resonant oscillator (when a parallel resonant quartz crystal is used).

The advantages of the second solution are low cost and low power consumption.

The aim of this application note is to provide a methodology to design an oscillator solution based on a quartz crystal operating in parallel resonance mode for the STR71x.

This document is split into two main sections. The first provides a brief description of both oscillator theory and the quartz characteristics while the second proposes an oscillator design and details the related components selection.

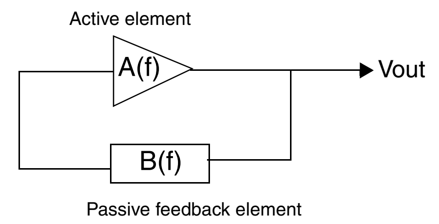
Contents

1 Oscillator theory

An oscillator consists of an amplifier and a feedback network to provide frequency selection.

The following figure shows the block diagram of the basic principle.

Figure 1. Oscillator principle



Where:

A(f) is the complex transfer function of the amplifier providing energy to the loop in order to keep it oscillating.

$$A(f) = |A(f)| \cdot e^{jf\alpha(f)}$$

B(f) is the complex transfer function of the feedback which is setting the oscillator frequency.

$$B(f) = |B(f)| \cdot e^{jf\beta(f)}$$

To oscillate, the following Barkhausen conditions must be fulfilled. The closed loop gain should be greater than 1 and the total phase shift of 360° is to be provided.

$$|A(f)| \cdot |B(f)| \geq 1$$

and

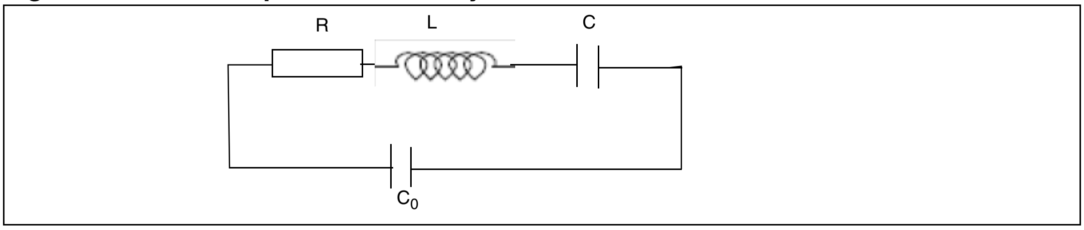
$$\alpha(f) + \beta(f) = 2\pi$$

In order to get the oscillator to start up, it needs initial electrical energy. Power-up transients as well as noise can supply the needed energy. However, the energy level should be high enough to trigger oscillation at the required frequency. Mathematically, this is represented by |A(w)|.|B(w)| >> 1 which means that the open loop gain should be much higher than 1. The time until steady oscillations are reached depends on the open loop gain.

2 Quartz crystal characteristics

A quartz crystal is a piezoelectric device transforming electrical energy to mechanical energy and vice versa. The transformation occurs at the resonant frequency. It can be modeled as follows:

Figure 2. Quartz equivalent circuitry



Where:

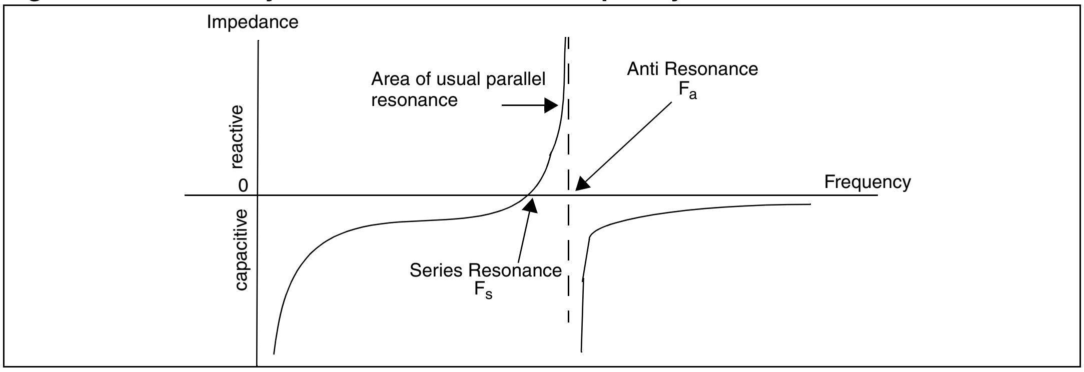
- **C_0** represents the shunt capacitance resulting from the capacitor formed by the electrodes and the parasites of the contacts.
- **L** (motional inductance) represents the vibrating mass of the crystal.
- **C** (motional capacitance) represents the elasticity of the crystal
- **R** represents the circuit losses.

Because R is normally negligible, the impedance of this circuitry is given by the following equation:

$$Z = \frac{j}{w} \times \frac{w^2LC - 1}{(C_0 + C) - w^2LCC_0}$$

The following figure represents the quartz reactance across its operating frequency:

Figure 3. Quartz crystal reactance across frequency



Two resonant frequencies can be calculated.

- The series-resonance frequency F_s is attained when the impedance Z approaches 0.

$$F_s = \frac{1}{2\pi\sqrt{LC}}$$

  The phase shift at the series resonance frequency is zero. At the series resonance, the impedance is minimal and the current flow is maximal.

- The anti resonance frequency F_a is attained when the impedance Z approaches the infinity."

$$F_a = F_s\sqrt{1+\frac{C}{C_0}}$$

The area between F_s and F_a is called the "usual parallel resonance" or simply "parallel resonance"

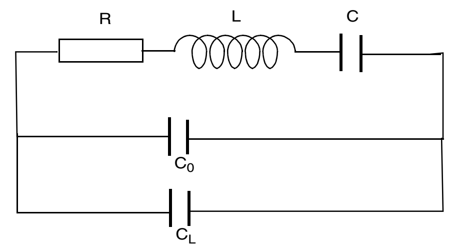
When the crystal operates in parallel resonance, its frequency F_p is between F_s and F_a and has the following expression

$$F_p = F_s\sqrt{1+\frac{C}{C_L+C_0}}$$

Parallel resonance means that a small capacitance called load capacitance C_L should be placed across the crystal terminals to obtain the desired operating frequency.

Figure 4 shows load capacitance with the crystal equivalent circuitry.

Figure 4. Load capacitance across a parallel resonant quartz



2.1 Frequency vs. mode

A crystal resonance can occur:

- at the F_a or F_p frequencies (formulas given earlier). This is the fundamental mode which is used for frequencies smaller than 30 MHz.
- at an odd multiple of the F_a or F_p (harmonics of F_a or F_p). These are the third, fifth, (...) overtone frequencies. This mode is used for frequencies above 30 MHz.

The crystal must be specified to operate at the desired frequency and on the desired overtone. One should never attempt to order a crystal operating at its fundamental frequency and operate it at an overtone frequency.

2.2 Direct drive

Quartz drive level is the power dissipated through the crystal while operating. It is usually expressed in terms of mW. Crystal units are specified to have a maximum drive level which changes with frequency and operating mode.

It is given by the following formula:

$$DriveLevel = RIr^2$$

where

Ir the current trough the crystal

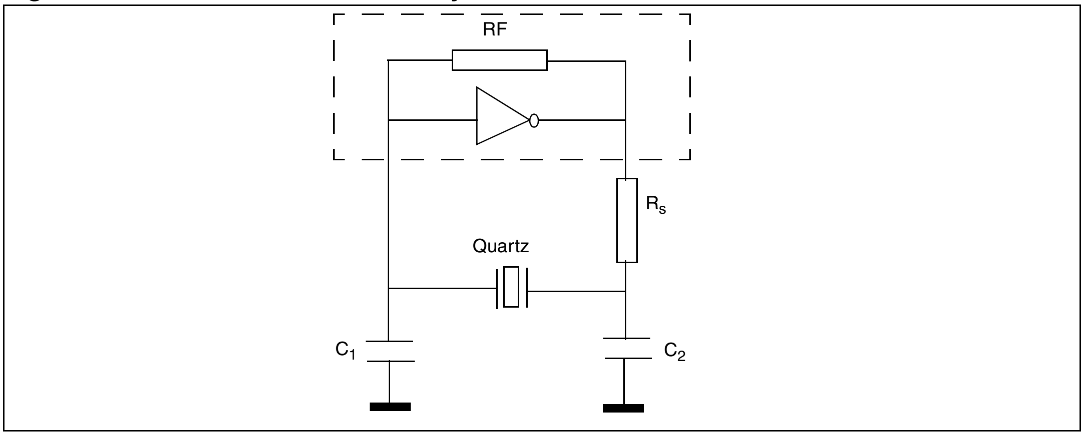
R is the maximum resistance value of the specified crystal.

The temperature has an impact on the crystal's frequency. The oscillator design should be tested in the application temperature range required.

3 Pierce oscillator design

Pierce oscillators are commonly used in applications because of their low consumption, low cost and their stability. They are based on the principle in the *Figure 5*.

Figure 5. Pierce oscillator circuitry

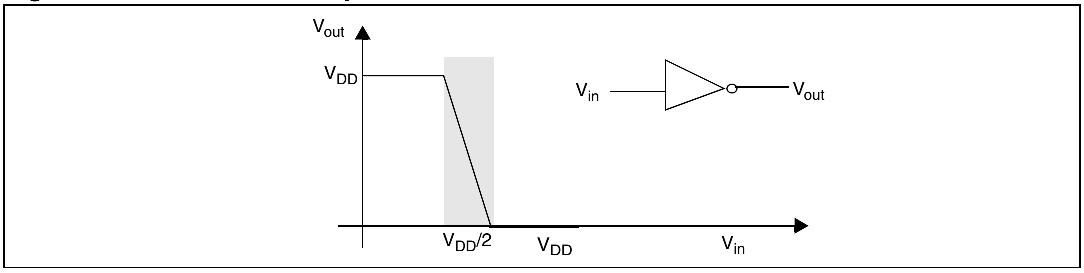


3.1 Amplifier element: 74V1GU04 ST inverter + feedback resistor

The amplifier is the active element in the oscillator design.

Basically, an inverter operating with a VDD power supply has the following response:

Figure 6. An Inverter Response



The transfer function of an inverter is non-linear. However, it acts as an amplifier only in the shaded area.

By biasing and operating the inverter near the maximum gain point, amplification is achieved. For this reason, a resistor is connected between the input and the output of the inverter.

For CMOS technology, typical values are between 1 MΩ and 10 MΩ. However, for TTL technology, typical values are around several hundred Ω.

In our example, the STMicroelectronics unbuffered inverter 74V1GU04 and a 2MΩ feedback resistor have been selected for the oscillator design.

The inverter creates 180° phase shift. In order to satisfy the Barkhausen's criteria phase condition for oscillation, a suitable feedback element should create the additional 180° phase delay. This is ensured by using a crystal operating at parallel resonance.

Once the crystal is selected according to the frequency and temperature range requirements of the application, a selection is necessary of the remaining components for the oscillator: C_1, C_2 and R_s. The section below assists in this process.

3.2 C_1 and C_2 capacitor selection

A parallel resonant crystal manufacturer specifies the load capacitance needed. This value is the load seen by the crystal which is in series with C_1 and C_2, including all parasites.

Load capacitance should be selected, at least to start with, per the data specified in the crystal datasheet. C_L has the following formula

$$C_L = \frac{C_1 \times C_2}{C_1 + C_2} + C_{stray}$$

where:

C_{stray} is the pin capacitance and board or trace PCB-related capacitance. Typically, it is between 2pF and 7pF. Please refer to the PCB hints in order to minimize its value.

In order to have a phase shift of 180°, C_1 and C_2 may have the same value.

As an example:

Assuming that C_{stray} = 5pF and that the crystal load capacitance is 15pF:

$C_1 = C_2$ = 20pF. The normalized value of 22pF is used.

Using 22pF as the C_L capacitance instead of 20pF slightly changes the parallel resonance frequency. However larger changes alter the resulting frequency. For frequency accuracy, the designer should select C_1 and C_2 values to stay as close as possible to the load capacitance specified by the manufacturer.

The oscillator start-up time depends on the crystal characteristics as well as C_1 and C_2 values.

If C_1 and C_2 increase, the start-up time increases. Therefore, C_1 and C_2 should be kept small but robust enough to provide adequate gain for start-up.

If the oscillator's start up time needs to be improved because of the application requirements, C_2 is increased compared to C_1. This causes greater phase shift across the crystal at power-up, which can speed the oscillator start up.

3.3 R_s resistor selection

R_s resistor is used in order to limit the output of the inverter so that the crystal is not over driven. The minimum value recommended depends on the crystal characteristics. Note that over-driving of the crystal can be observed on the oscillator output signal (where the signal is non-symmetrical or is oscillating at the harmonic frequency). Crystal over-driving shortens its life and in some cases, permanently damages it.

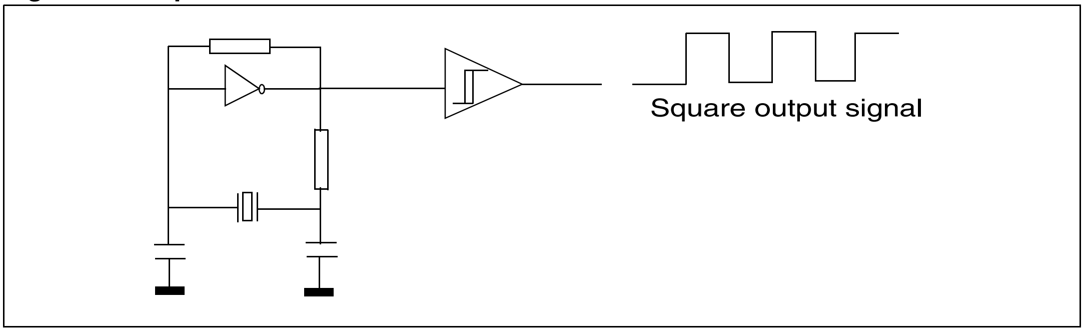
Ideally the inverter provides 180° phase shift, but the inherent delay of the inverter provides additional phase shift. In order to ensure the total 360° shift delay, R_s can be used to decrease the shift delay in the feedback loop.

R_s and C_2 form a voltage dividing circuit. Acceptable results can be reached by choosing the value of R_s equal to the C_2 capacitive reactance.

The recommended way to optimize R_s is to first choose C_1 and C_2 values as explained earlier and connect a potentiometer in place of R_s. Its initial setting should be set to be approximately equal to C_2 capacitive reactance, and then adjusted if required until an acceptable output and crystal drive level are found. The output signal should also be in line with the minimum and maximum V_{IL} and V_{IH} voltages applied on the STR71x CK pin.

To have a square signal, a schmidt trigger device can be added at the inverter's output.

Figure 7. Square wave oscillator



The STR71x device embeds an on-chip schmidt trigger on the CK pin so is not needed in this example, thus making the solution more cost-effective.

The designed oscillator is mounted on an STR7 generic board. The STR71x PLL is configured to generate 48 MHz from the 16-MHz oscillator output and a GPIO pin level is toggled before and after PLL lock. This test is passed successfully.

For design robustness, the signal obtained should be tested in a worst case scenario:

- Application at highest temperature and lowest V_{DD} voltage.
- Application at minimum temperature and highest V_{DD} voltage.

4 16-MHz oscillator example

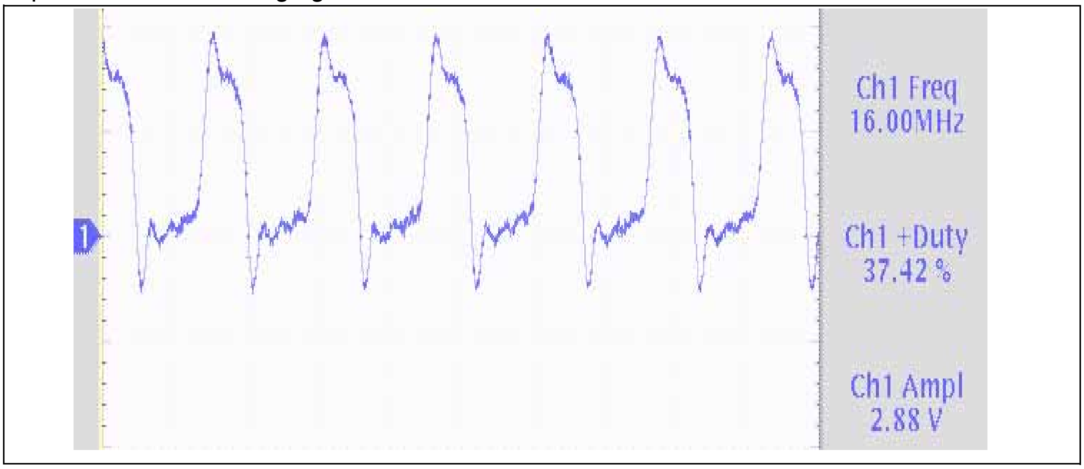
In this section, the steps and guidelines described in the previous section are put into practice in order to design a 16-MHz oscillator.

The first step concerns the discrete components selection:

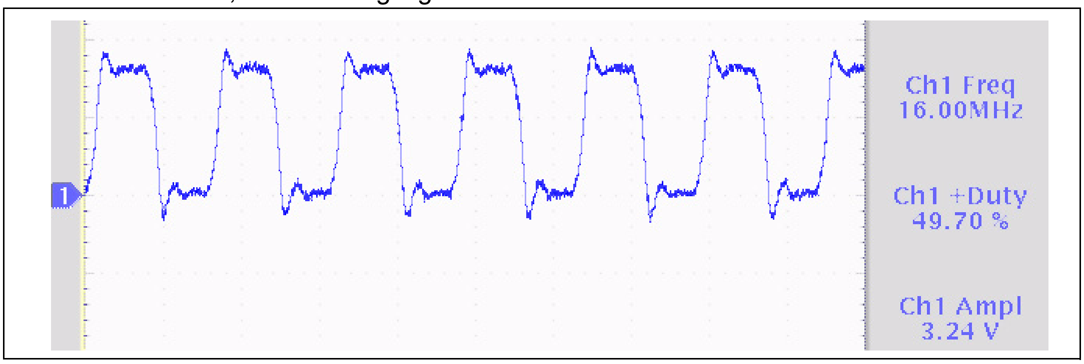
- The STMicroelectronics non-buffered inverter 741VGU04STR operating with VDD = 3.3 is selected for this application. In order to make the inverter act as an amplifier, a 2MΩ resistor is put between its input and output pads (Rf = 2M)
- The 16-Mhz quartz CQ is selected. C1 and C2 are selected according to the Quartz specification. According to the quartz characteristics, a loading capacitor of **20pF** makes the quartz operate at its16 MHz parallel frequency. Theoretically, if we consider an 8pF stray capacitance, C1 and C2 are calculated using the formula on *Section 3.2 on page 8*.
  C1 = C2 = 24pF.

  The standard value of 22pF is taken for both C1 and C2.

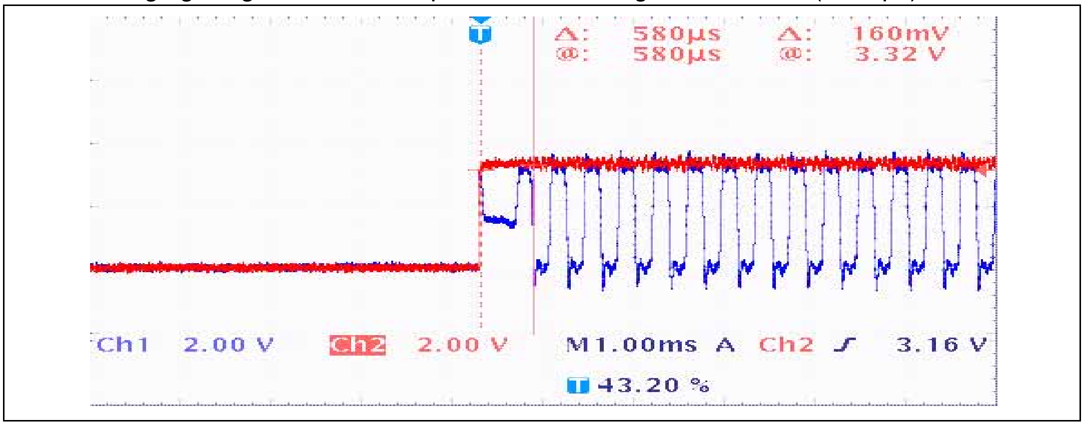
After soldering these components without the Rs resistor, the oscillator output signal is captured in the following figure.



The signal obtained is not symmetric. Therefore, an Rs resistor is put between the inverter output and the quartz. To start, a potentiometer is put between these two nodes and with a variable Rs resistor, the following signal is obtained for Rs = 1 KΩ.

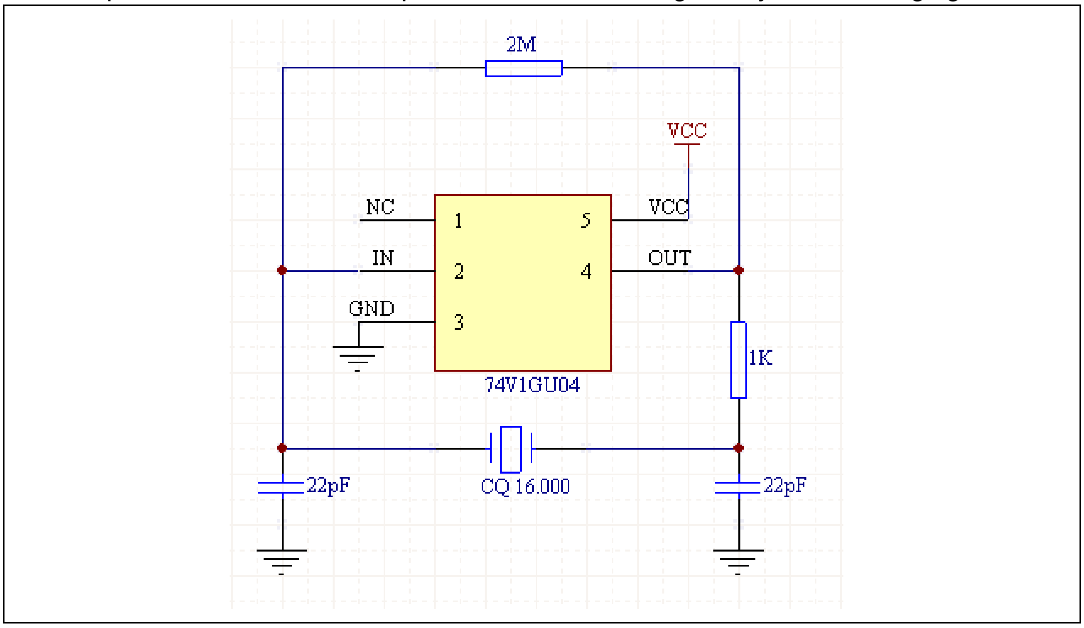


The following figure gives the start-up time of the designed oscillator (~580µs).



With Ch2 as VDD and Ch1 as the output signal.

The complete schematic of the implemented oscillator is given by the following figure.



In the next section, a number of PCB hints are given to reduce the noise that can affect the oscillator

5 PCB hints

This section gives some design guidelines that must be respected for good oscillator design.

- A large stray capacitance and large inductances must be kept to a minimum to avoid an undesired mode of oscillation, and problems with startup. In addition, high frequency signals should be avoided near the oscillator circuitry.
- Trace lengths should be kept as short as possible. Ground plans should be used to isolate signals and reduce noise.
- Use decoupling capacitors between each V_{DD} and its nearest V_{SS} to smooth noise.

6 Revision history

Table 1. Document revision history

Date	Revision	Changes
02-Apr-2007	1	Initial release.

Please Read Carefully:

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com