

Integrating TIMEKEEPER[®] and real-time clock supervisor functions

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Introduction

STMicroelectronics' TIMEKEEPER supervisors include real-time clock and NVRAM supervisor functions which enable users to easily implement RTC and battery-backed SRAM functions within their designs. With the RTC and battery switchover on the same chip, only a single coin cell battery is needed to maintain both the RTC and the NVRAM.

These devices include other helpful supervisory functions such as power-on-reset/low-voltage-detect, watchdog, power-fail comparator and battery monitor.

Integrating these many features into one device helps users to develop robust systems with minimal cost and board space.

Table 1. TIMEKEEPER supervisory functions

Device	Package	Bus	Battery switchover	Chip-enable gating	Power-on reset/ Low-voltage detect	Tamper detect inputs	Alarm	Watchdog	Squarewave output	Dedicated 32 KHz output	Manual reset inputs	Power-fail comparators (PFI-PFO)	Battery monitor
M41ST85WMX	Embedded crystal SOX-28	400 kHz I ² C	✓	✓	✓		✓	✓	✓		2	1	✓
M41ST85WMH	SNAPHAT ⁽¹⁾ SOH-28												
M41ST87WMX	Embedded crystal SOX-28	400 kHz I ² C		✓							2		
M41ST87WSS	SSOP20		✓	No	✓	2	✓	✓	✓	✓	1	2	✓
M48T201Y/V	SNAPHAT ⁽¹⁾ SOH-44	Parallel 8-bit	✓	✓	✓		✓	✓	✓		2		✓

1. See battery and crystal options for Timekeeper supervisors on www.st.com.

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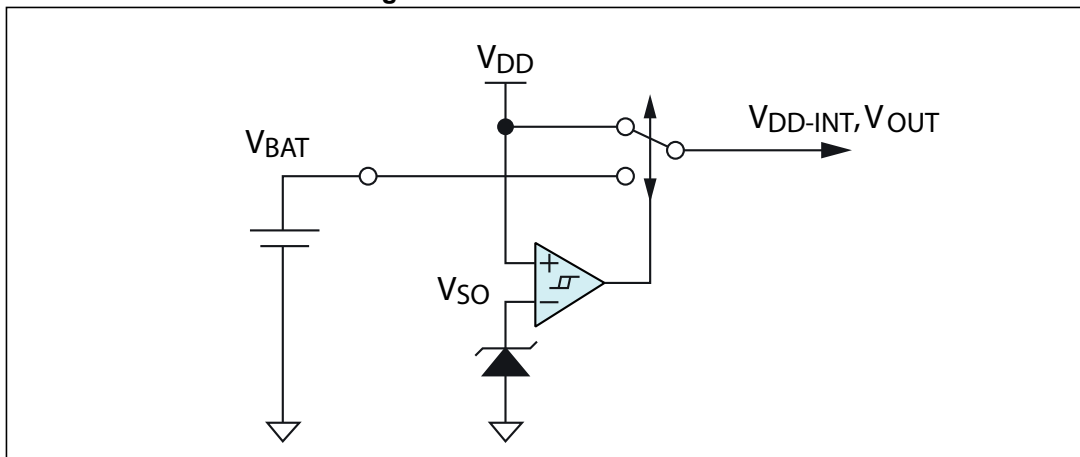
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1 Battery switchover and chip-enable gating (write protection)

The battery switchover mechanism is a key feature of real-time clocks and battery-backed SRAMs (ie. NVRAMs). In a typical RTC or NVRAM application, when V_{DD} fails, it is paramount that the device be seamlessly switched to the backup battery to prevent loss of data or corruption of the RTC contents. The switchover circuit must detect V_{DD} falling and connect the RTC/SRAM to the backup battery (V_{BAT}) without ever letting the voltage at the RTC/SRAM fall too low. Thus the switchover mechanism must have a switchover threshold higher than the minimum voltage tolerated by the load. Furthermore, the switchover circuit should provide a gating signal to cut off access to the load. This signal write-protects the RTC/SRAM when V_{DD} fails.

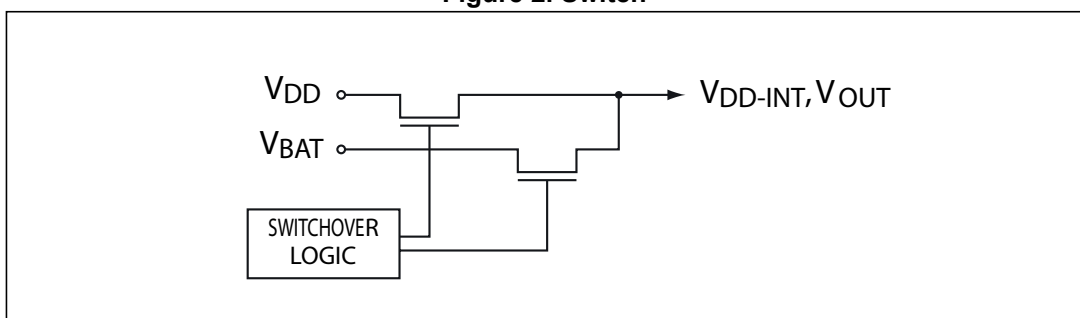
A basic switchover function is shown below. When V_{DD} falls below the switchover threshold, V_{SO} , the load is switched to V_{BAT} . The switch output supplies both the internal circuits (V_{DD-INT}) and the external load (V_{OUT}).

Figure 1. Switchover function



The actual switch is implemented using FETs, and is wired as shown below.

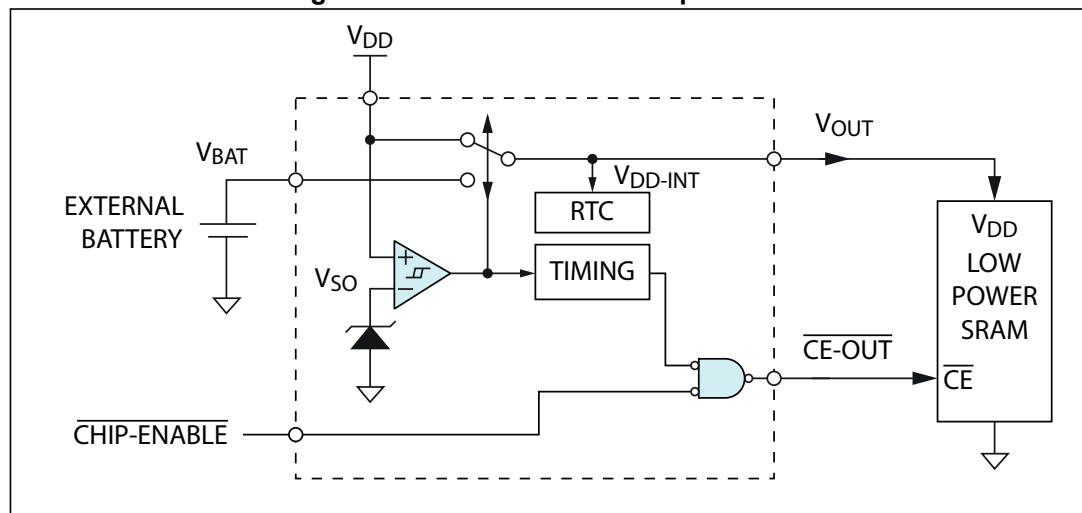
Figure 2. Switch



In a backup application, the hookup would be similar to that shown below. The switchover circuit provides power to the external SRAM through V_{OUT} , which supplies both active and backup current to the load. When V_{DD} fails, the switchover automatically connects the battery to the external SRAM and to the internal circuits of the TIMEKEEPER supervisor including the real-time clock. At the same time, the chip-enable is gated off to the external low-power SRAM thereby write-protecting it.

When V_{DD} comes back up, the timing block ensures that the LPSRAM remains write-protected for a short time afterward, typically 40 to 200 milliseconds (the same as the t_{REC} interval).

Figure 3. Switchover and write protection

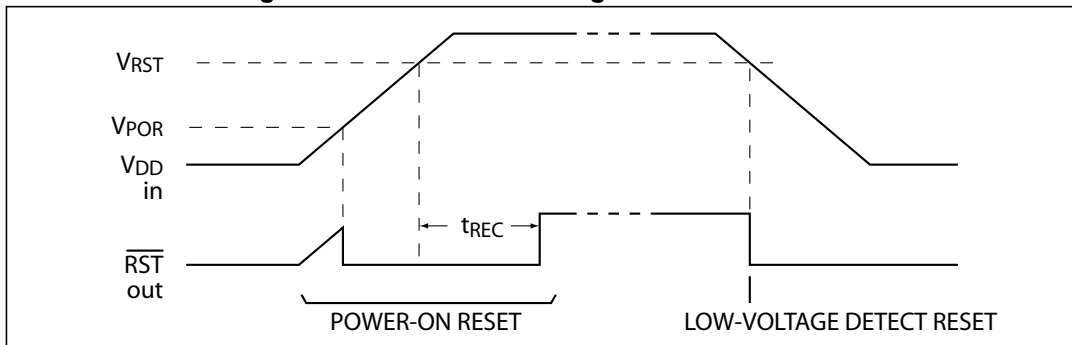


For typical battery-backed SRAM applications, the low-power SRAM needs to have a standby/backup current on the order of a few microamps or less in order to support a useful battery life. For example, with a 120 milliamp-hour battery and a load of 1 microamp for the SRAM and 0.5 microamps for the RTC, a backup life of over 9 years is expected.

2 Power-on reset and low-voltage detect

The basic function of POR/LVD is to hold the system in reset whenever the system voltage is out of the preferred operating range. This means that the POR/LVD reset output is asserted when V_{DD} is ramping up and also when it is ramping down.

Figure 4. POR and low-voltage detect waveforms



As shown in the figure above, when V_{DD} rises above the V_{POR} threshold, \overline{RST} is actively driven low. It stays low until V_{DD} has stayed above V_{RST} for a period of time, labeled t_{REC} . The length of t_{REC} is in the range 40 to 200 milliseconds. Configuration bits in the TIMEKEEPER supervisors allow the user to specify a narrower t_{REC} range of 96-98 milliseconds.

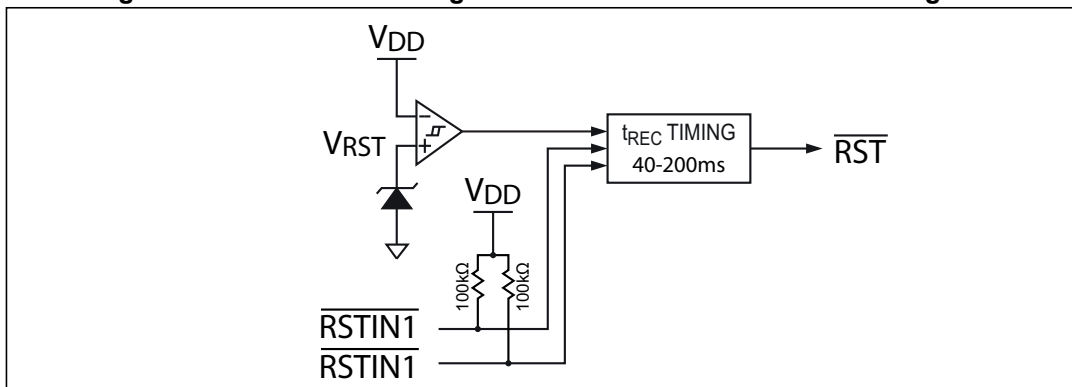
V_{RST} varies with device type, and includes options such as 4.35, 2.9 and 2.62 volts, as well as others. Consult the applicable datasheet for more details.

2.1 Reset inputs

The POR/LVD circuits also include external reset input signals. These active low inputs have built-in pull-up resistors and can be used to implement a push-button reset function, or to gate in another reset signal from another source on the customer board. The timing details for these varies, but the basic concept is that when the input is asserted, the \overline{RST} output will go low and stay low for a period the specified t_{REC} interval, minimum.

A diagram of the POR/LVD circuit is shown below. In essence, the two reset inputs are logically OR'd with the comparator output.

Figure 5. POR and low-voltage detect circuit with external reset signals

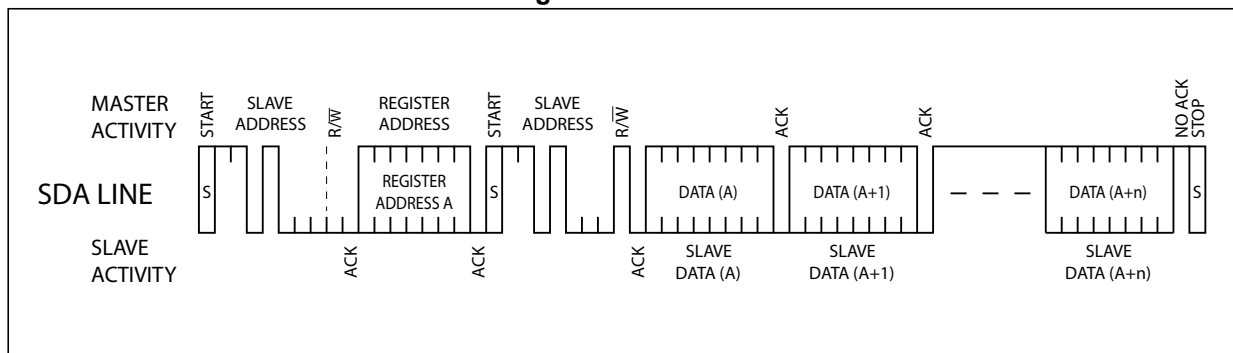


3 System interface

The M41ST85W and M41ST87W devices each incorporate a 400kHz I²C interface (Inter-Integrated Circuit). This popular two-wire interface provides access to the clock and calendar functions as well as the status and control registers and the battery-backed SRAM on board the chips. Both devices support address auto-increment – a single-byte write to the address register can be followed by multiple-byte data reads (or writes) of the internal registers. The first byte read (written) is from the address pointed to by the address register, then the device automatically increments the address to point to the next data register such that the next byte transferred is from (to) that register.

As shown in the read example below, each successive data byte transferred comes from the next higher address.

Figure 6. I²C read

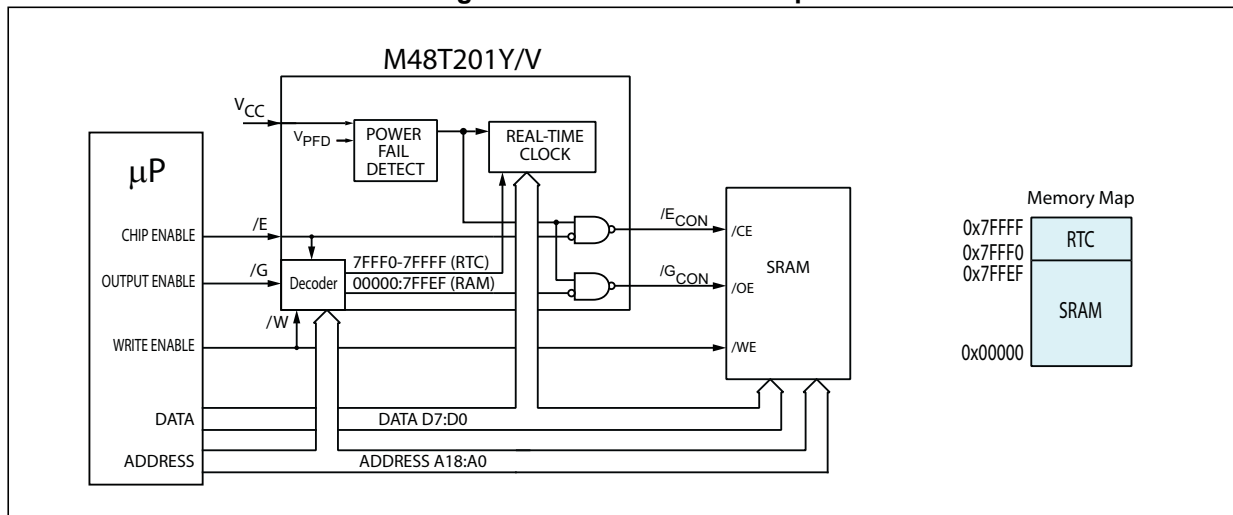


Auto-increment allows the application to move data faster because the register address only needs to be sent once for multiple data byte transfers.

3.1 Parallel access

The M48T201Y/V connects to the processor in much the same manner as an SRAM (or any other read/write, random access memory). 19 address lines and 8 data lines comprise the essential connections while three other lines provide the timing and read/write control. All accesses to the RTC registers (and the SRAM contents) have 8 bits of data being transferred simultaneously, in parallel.

Figure 7. M48T201Y/V hookup



The M48T201Y/V memory maps the clock/calendar registers into the address space of an external SRAM. For example, if used with a 512K-byte SRAM, the upper 16 bytes of the SRAM space (addresses 0x7FFF0 to 0x7FFFF) will actually be the clock/calendar registers while the lower 524,272 bytes will be the SRAM (addresses 0 to 0x7FFEF).

Compared to serial interface, the parallel interface has the advantage that the data can be transferred much more quickly between the processor and the device. For example, 8 bytes can be transferred to/from the M48T201Y/V in approximately 1.6 micro-seconds. (This assumes 100 ns for each data byte transferred plus 100 ns of instruction fetch prior to each data byte.) For the 400 kHz I²C bus, that same sequence, using address auto-increment, would still take 255 μs, over 100 times as long.

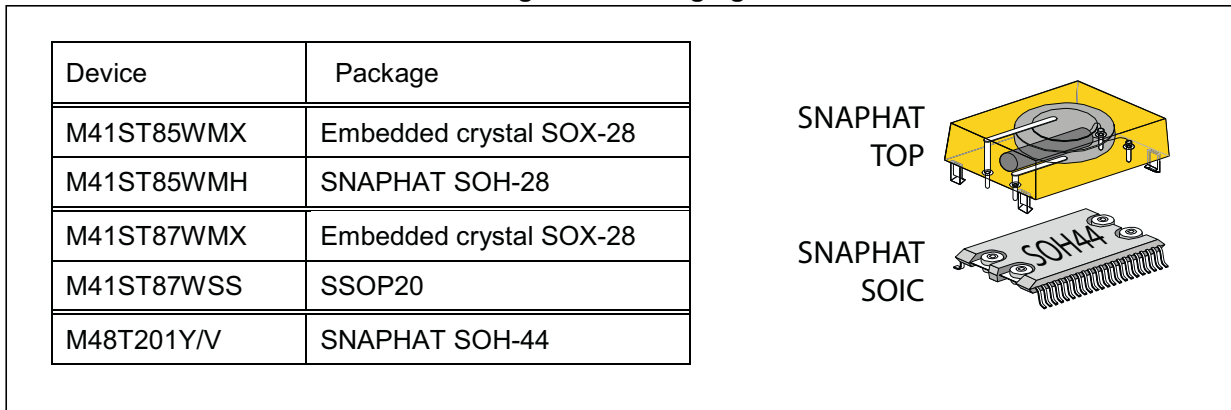
4 Packaging

TIMEKEEPER supervisors use IC packages based on industry standard packaging technology. The M41ST87WSS uses a common 20-lead shrink, small outline package (SSOP-20). The user connects a battery and crystal to this device.

For the M41ST85WMX and M41ST87WMX, the crystal is embedded into an otherwise common 300 mil (7.62 mm) 28-pin small outline IC package (SOIC). The user connects an external battery with these devices.

ST's flagship package is the SNAPHAT SOIC. This has the same envelope as an ordinary 330 mil (8.38 mm) SOIC. The 28-pin version (SOH-28) has the same footprint as well, but the 44-pin version tightens the spacing to squeeze in 44 pins while maintaining the same overall outline as the 28-pin version. The advantage of this packaging is that the battery and crystal are contained in a mating hat which sits atop the IC package. Two extra connections on each end of the IC package provide the contacts for the crystal and battery contained in the SNAPHAT top. The same hat fits both the SOH-28 and the SOH-44.

Figure 8. Packaging



5 Tamper detection

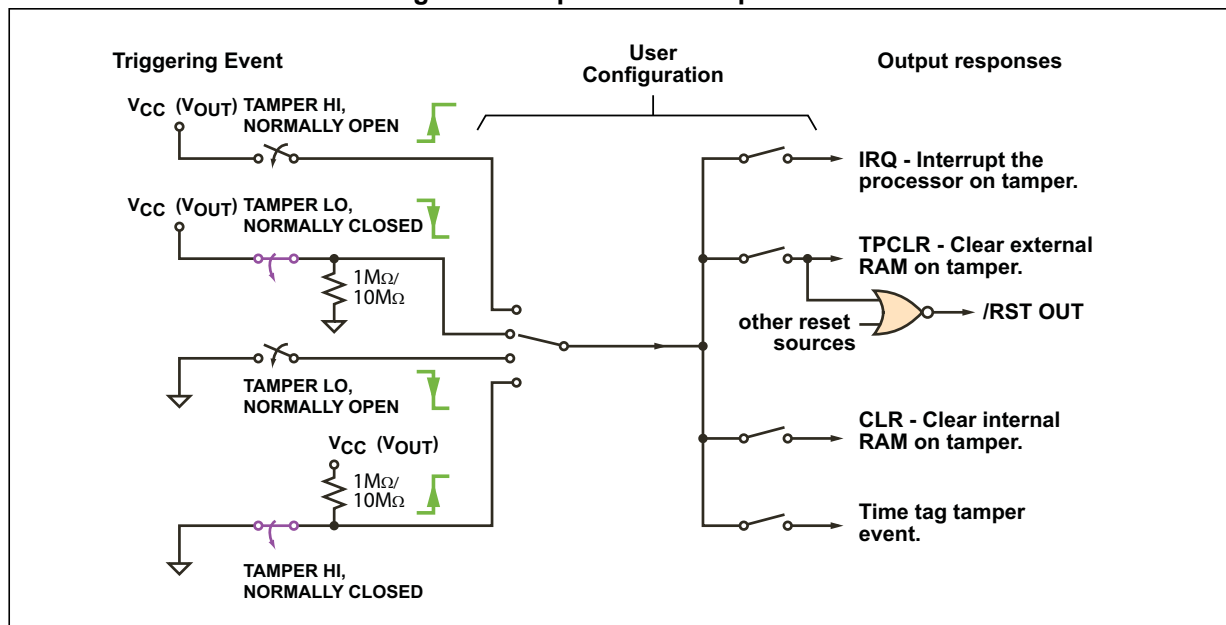
In applications where high security is critical, tamper detection provides a means of ensuring that data is not stolen. With battery-backup protection, the tamper detect function can be used to trigger the erasure of data whenever a physical breach is detected, even when the system is not powered. Furthermore, a time tag of the event is recorded providing additional evidence of the intrusion.

The tamper detect inputs can be used to detect a switch opening or closing, and then the device can respond in a variety of ways as configured by the user.

As shown below, along with whether the switch opens or closes, the user can select the input polarity as well. Also, for the normally closed cases, the user can select between 1M and 10M resistors in order to reduce battery draw. Not shown in the drawing, the user can also select whether the input is continuously monitored or periodically sampled, to save power, for the two normally closed cases.

On the output side, the user can select among four different responses to the tamper event. Any combination of these options may be selected.

Figure 9. Responses to tamper event



Because the tamper detect function draws so little current, it can readily be battery-backed. This ensures that the tamper function continues to operate in the event of a power loss. Intruders seeking to bypass the tamper detection cannot do so by removing system power. Thus sensitive data will remain protected even in the absence of system power.

6 Alarm

The alarm function is much like the alarm on an ordinary alarm clock. The user sets the time for the alarm to occur, and the device generates an interrupt when the current time matches the alarm time. The user can specify not only the hours, minutes and seconds of the alarm event, but also the month and date (day-of-month) such that the alarm can be configured to only occur once per year. Other configuration options allow the user to select the alarm to occur once per month, once per day, once per hour or every second.

When an alarm interrupt is asserted, the application clears the interrupt by reading the device's flags register which causes the interrupt to de-assert.

7 Dedicated 32.768 kHz output

Many oscillator based devices include phase-locked loop clock synthesis circuits. These replace or augment the oscillators commonly used. Ordinary 32.768 kHz watch crystals are reasonably accurate while providing significant cost reductions over higher frequency AT-cut crystals. Typically, in microprocessor applications, the PLL clock synthesis generates a high frequency signal derived from the 32.768 kHz oscillator. This higher frequency signal provides the timing reference to run the processor without needing the higher cost AT-cut crystal.

Since real-time clock devices already have 32.768 kHz oscillators, users can further reduce system costs by using the RTC's oscillator to drive the processor's PLL input thereby eliminating the duplicate 32.768 kHz crystal. The M41ST87 includes a 32.768 kHz dedicated output for just that application.

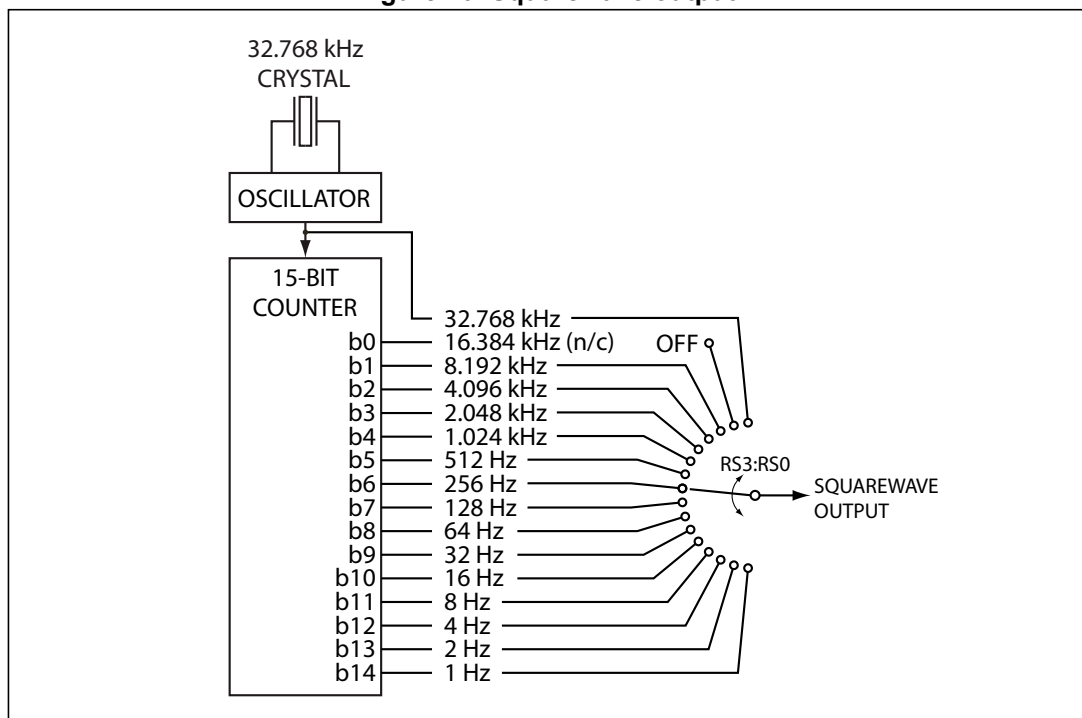
This output is enabled at first power-up and is present as long as V_{CC} remains above the switchover threshold, V_{SO} . It can also be disabled by clearing the non-volatile control bit, 32kE, to 0.

8 Programmable squarewave output

By connecting the 32.768 kHz oscillator signal to a 15-bit binary counter, 15 lower frequency signals can be derived. Each tap of the counter outputs a signal half the frequency of the tap above it. The result is that frequencies all the way down to 1 Hz are generated. These are then fed into a switch under control of the application. The four bits RS3:RS0 control which of the signals drives the squarewave output pin.

Note that the 16.384 kHz signal is not available. Only 15 of the 16 frequencies are available, with the 16th position being OFF instead of 16.384 kHz.

Figure 10. Squarewave output



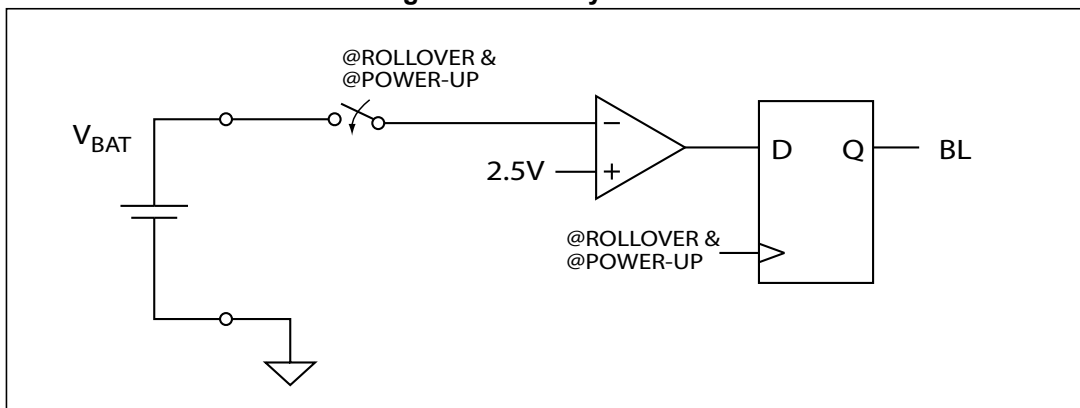
9 Battery monitor

To help maintain non-volatility, the battery monitor function can inform the application that the battery needs to be replaced before any data is lost.

The battery monitor circuit checks the battery every night at midnight (rollover) and every time the device powers up from backup mode. The battery is compared to 2.5 V and the BL bit (battery low) is updated each time this occurs.

In some applications, users need to force a BL update. A common trick to do this is to store the current time, then write the time to 1 second before midnight (11:59:59pm), wait 2 seconds, then restore the previously saved time (plus 2 seconds). This will update the BL bit without needing to power-cycle the device.

Figure 11. Battery monitor

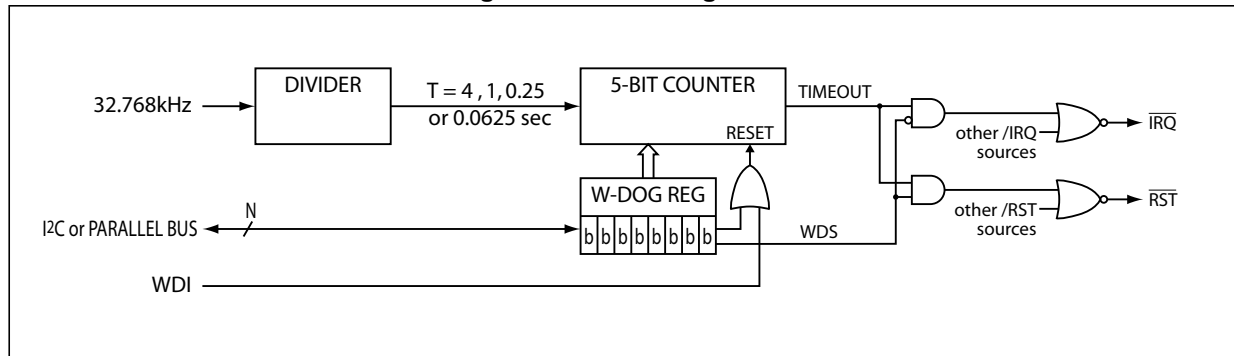


10 Watchdog timer

The essential function of the watchdog timer is to reset the system whenever too much time has elapsed since the last reset of the watchdog timer. The usual application is for the software to occasionally reset the watchdog timer on a regular basis and, when that does not occur, it is assumed the software is hung up and must be re-initialized in order to recover. So the watchdog timer's output is steered to the system reset signal (\overline{RST}) or to an interrupt (\overline{IRQ}). As long as the application routinely resets the timer, then no timeout will occur. But if the software somehow gets hung, then the watchdog will time out and cause the reset (or interrupt) to occur thereby prompting the system to resume operation.

The M48T201Y/V, M41ST85W and M41ST87W all employ the same basic watchdog. Its timer is reset whenever the WDI pin is toggled, or whenever the application writes to the watchdog register via I²C (or parallel bus in the case of the M48T201Y/V). The user can select one of four clock periods to drive the 5-bit counter. The programmable timeout period ranges from 1/4 second to 124 seconds. Please consult the specific device datasheet for more information.

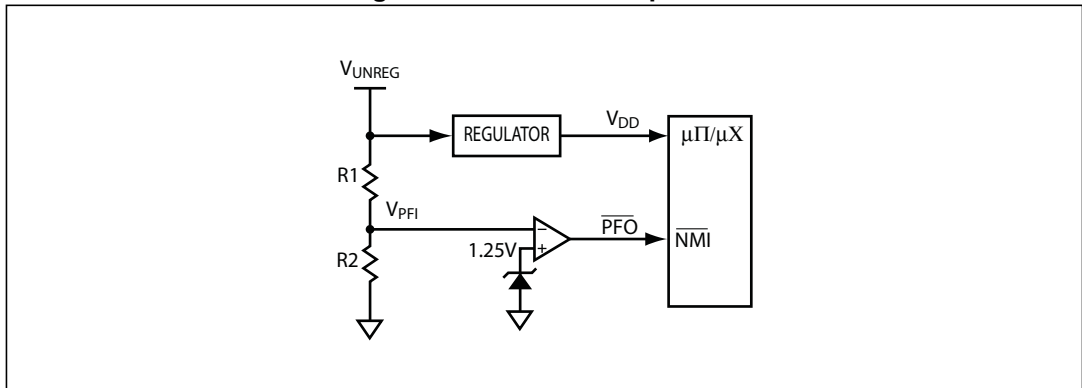
Figure 12. Watchdog timer



11 Power-fail comparator (PFI-PFO) - early power-fail warning

In most RTC/NVRAM applications, the battery switchover and write-protect timing is sufficient to maintain the non-volatile data and the timekeeping function without needing any advanced warning; whenever the system power fails, the device automatically and simultaneously switches to backup mode.

Figure 13. PFI-PFO comparator



But some applications, at power-fail, require additional time to store away critical data into NVRAM and then gracefully shut down. The PFI-PFO comparator (power-fail in / power-fail out) can be used to generate an advanced warning that power may soon fail. By monitoring the system power upstream of the regulator, the system can determine when the unregulated voltage has fallen critically low and send an interrupt to the microprocessor. By measuring the unregulated voltage over time, the user can characterize the typical failure profile and choose R1 and R2 accordingly.

12 Summary

Users will find that ST's family of TIMEKEEPER supervisors not only make it easy to implement NVRAM and RTC functions in any system, but that they also include many other supervisor features which make the system more robust while providing a compact and cost-effective solution.

13 References

- *AN1336*: Power-fail comparator for NVRAM supervisory devices.

14 Revision history

Table 2. Document revision history

Date	Version	Changes
07-May-2015	1	Initial release

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