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Application note

STM32L5 Series to STM32U575/585 migration guide

Introduction

The designers of STM32 microcontroller applications must have the possibility to easily replace one microcontroller type with another one from the same product family or products from a different family. The reasons for migrating an application to a different microcontroller can be for example:

- to fulfill higher product requirements, extra demands on memory size, or an increased number of I/Os
- to meet cost reduction constraints that require to switch to smaller components and shrink the PCB area

This application note details the steps required to migrate from a design based on a STM32L5 Series device (named STM32L5 in this document) to an application based on one of the STM32U575/585 MCUs.

This document provides guidelines for the hardware and the peripheral migration. To better understand the information inside this application note, the user must be familiar with the STM32 microcontroller family.

1 STM32U575/585 overview

The STM32U575/585 devices are ultra-low-power and security MCUs, with enhanced efficiency and performance, such as:

- up to 2 Mbytes of Flash memory accelerated by instructions/data caches
- up to 786 Kbytes of RAM with optional ECC and 2 Kbytes of backup SRAM

The STM32U575/585 reuse the same embedded Arm® Cortex®-M33 32-bit core than the STM32L5. This core runs at 160 MHz for STM32U575/585 versus 110 MHz for STM32L5. This core provides improved security features thanks to the ultra-low-power Arm® TrustZone® for Armv8-M, and thanks to the ST instruction/data caches (ICACHE and DCACHE) that support both internal and external memories.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

The STM32U575/585 include a larger set of peripherals with more advanced features compared to the STM32L5, such as the ones listed below:

- Power consumption
  - Optimized power consumption in dynamic, using DC/DC and LDO in parallel (on-the-fly selection)
  - Optimized power consumption in low-power modes:
    - DMA and autonomous peripherals available in Stop mode: LPDMA (low-power DMA featuring one master port) functional in SmartRun domain (SRD). SRD architecture relies on a DMA allowing autonomous operation during low-power modes down to Stop 2.
    - Possibility to power on or off some SRAM banks and to keep them in low-power modes
    - Timers running in Stop mode with input capture mode
    - Optimized RTC consumption
    - Advanced 14-bit ADC and ultra-low-power 12-bit ADC
- Security: upgraded features versus STM32L5
  - AES and PKA (public key accelerator), side attack resistant (by hardware)
  - HUK (hardware unique key) to get a secure storage resistant to logical, side and physical attack
  - Life-cycle/RDP (readout protection): possibility to enable RDP regression with password
  - TrustZone
  - Active tampering
  - Temperature, voltage and frequency protection monitoring for tamper detection
  - PKA intended for the computation of cryptographic public key primitives, specifically those related to RSA, Diffie-Hellmann or ECC (elliptic curve cryptography) over GF(p) (Galois fields). To achieve high performance at a reasonable cost, these operations are executed in the Montgomery domain.
  - OTFDEC (on-the-fly decryption engine) to decrypt on-the-fly the AHB traffic based on the read request address information
- System
  - Performance
    - Cortex-M33 at 160 MHz
    - 100 k cycles for 256 Kbytes of Flash memory (the rest at 10 k cycles).
    - Programmable ECC for the SRAM
  - New coprocessors
    - FMAC and CORDIC (mathematics accelerators coprocessors)
    - Instruction and data caches for internal and external memory (ART Accelerator)
    - Multi-function digital filters with advanced features

Note: This document only manages the differences between STM32U575/585 and STM32L5 for the common features. The new features in STM32U575/585 are not covered. The detailed list of available features and packages for each product is available in the respective product datasheet.

1.1 Memory availability

The STM32U575/585 embed more memory than the STM32L5 as shown in the table below.

Table 1. Memory size on STM32L5 and STM32U575/585

Products	Flash memory		RAM size (Kbytes)					Comment
	Size (Kbytes)	Bank	SRAM1	SRAM2	SRAM3	SRAM4 (SRD)(1)	Backup SRAM	
STM32L552xx	Up to 256	Single/ dual	192	64	-	-	-	Without hardware crypto
STM32L562xx	512							With hardware crypto
STM32U575xx	2048	Dual			512	16	2	Without hardware crypto
STM32U585xx								With hardware crypto

1. *SmartRun domain.*

1.2 System architecture differences between STM32U575/585 and STM32L5

Both STM32U575/585 and STM32L5 embed high-speed memories, a flexible external memory controller (FSMC) for static memories, one (STM32L5) or two (STM32U575/585) Octo-SPI Flash memory interfaces, and an extensive range of enhanced I/Os and peripherals connected to APB buses, AHB buses and a 32-bit multi-AHB bus matrix.

The bus matrix provides access from a master to slave, enabling concurrent access and efficient operation when several high-speed peripherals work simultaneously.

In addition, the STM32U575/585 connect more masters and slaves to the bus matrix than the STM32L5: SDMMC DMA master and two Octo-SPI Flash memory interfaces. The STM32U575/585 also embed more peripherals in the new low-power SRD (SmartRun domain) connected to AHB3 and APB3 internal buses.

The figures below detail the STM32U575/585 and STM32L5 system architecture.

Figure 1. STM32U575/585 system architecture

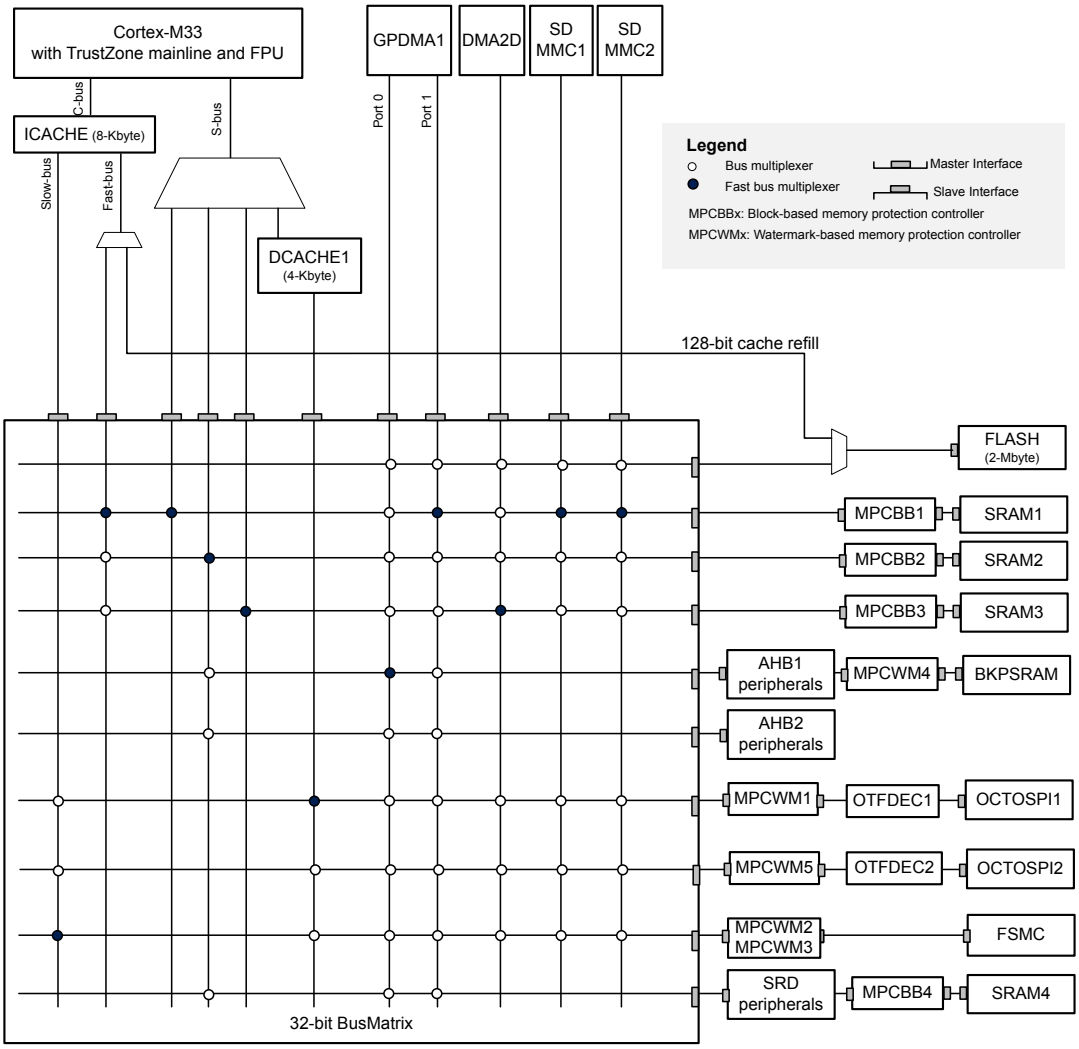
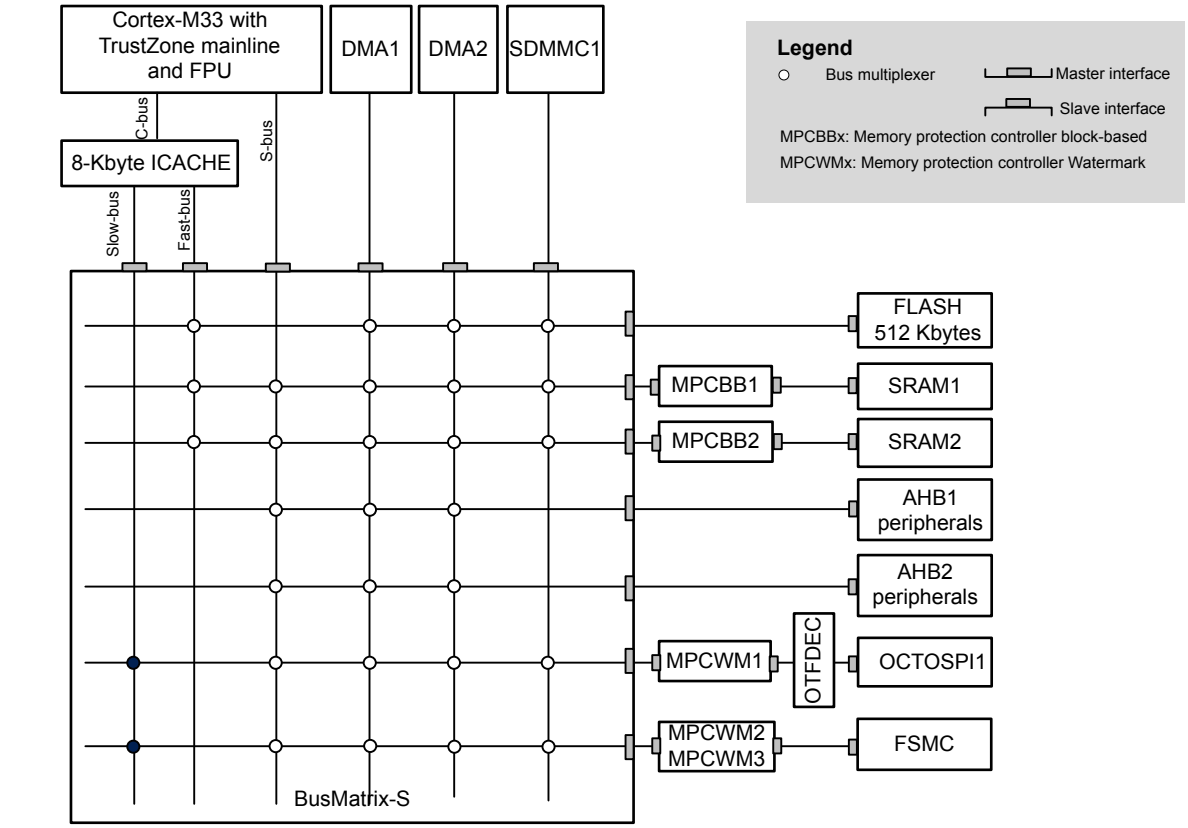


Figure 2. **STM32L5 system architecture**



- When remapped by ICACHE

The STM32U575/585 architecture features a 32-bit multilayer AHB bus matrix that interconnects up to eleven masters and up to ten slaves (see the tables below).

Table 2. Masters connected to AHB bus matrix of STM32L5 and STM32U575/585

AHB bus matrix masters	Fast C-bus ICACHE	Slow C-bus ICACHE	S-bus	DCACHE1 S-bus	GPDMA1	DMA2D	SDMMC	Total
STM32U575/585	1	1	3	1	2(1)	1	2	11
STM32L5	1	1	1	-	2 (DMA1, DMA2)(2)	N/A	1	6

1. *GPDMA1 is an advanced DMA module (16 channels), with two master ports connected to the bus matrix.*
2. *Each DMA (8-channels) module is connected separately to the bus matrix.*

Table 3. Slaves connected to AHB bus matrix of STM32L5 and STM32U575/585

AHB bus matrix slaves	Internal Flash memory	SRAMs	AHB1 periph.	AHB2 periph.	AHB3 SRD	OCTOSPI	FSMC	Total
STM32U575/585	1(1)	3	1(2)	1	1(3)	2	1	10
STM32L5	1	2	1	1	-	1	1	7

1. *In addition to this master port, the STM32U575/585 embed a 128-bit cache refill bus that connects the Flash memory to the ICACHE. This allows optimized core execution thanks to the direct access to embedded Flash memory.*
2. *Including BKPSRAM, APB1 and APB2 peripherals.*
3. *AHB3 peripherals, SRAM4 and APB3 peripherals.*

2 Hardware migration

The STM32U575/585 offer seven packages from 48 to 169 pins and two versions of pinout:

- without internal SMPS: fully compatible with STM32L5 except on VCAP pin for decoupling capacitors, used by the LDO to regulate the power supply
- with internal SMPS: UFBGA132 packages are fully compatible with STM32L5, but QFP packages have six pins of differences needed by the internal SMPS.

The SMPS step-down converter is available only on the STM32U5xxxxQ and STM32L5xxxxxxQ specific products.

Note: The STM32L5xxxxxxP products have an external SMPS power supply. They are not compatible with STM32U575/585 and not checked in this application note. For more details on the pinout refer to the product datasheets.

The table below lists the available packages without SMPS on the STM32U575/585 compared with similar packages of STM32L5. It lists also the pinout compatibility and differences between these packages.

Table 4. Packages without SMPS on STM32L5 and STM32U575/585

Package (size in mm x mm)	STM32U575/585 versus STM32L5	Pinout differences		
		Pin number	Pin name (U5)	Pin name (L5)
UQFP48 (7 x 7) LQFP48 (7 x 7)	• Compatible with one difference on pin 22 (the other pins are the same) • No PB11 in STM32U575/585 packages	22	VCAP	PB11
LQFP64 (10 x 10)	• Compatible with one difference on pin 30 (the other pins are the same) • No PB11 in STM32U575/585 packages	30	VCAP	PB11
LQFP100 (14 x 14)	• Compatible with one difference on pin 48 (the other pins are the same) • No PB11 in STM32U575/585 packages	48	VCAP	PB11
LQFP144 (20 x 20)	• Compatible with one difference on pin 70 (the other pins are the same) • No PB11 in STM32U575/585 packages	70	VCAP	PB11
UFBGA132 (7 x 7)	• Compatible with one difference on ball L10 (the other balls are the same)	L10	VCAP	VSS
UFBGA169 (7 x 7)	• Not available for STM32L5 • New STM32U575/585 specific ballout	-	-	-

The table below lists the available packages with SMPS on the STM32U575/585 compared to similar packages of STM32L5. It lists also the pinout compatibility and differences between these packages.

Table 5. Packages with SMPS on STM32L5 and STM32U575/585

Package (size in mm x mm)	STM32U575/585 versus STM32L5	Pinout differences		
		Pin number	Pin name (U5)	Pin name (L5)
UQFP48 (7 x 7) LQFP48 (7 x 7)	Compatible with differences on six pins related to internal SMPS power supply	20	VLXSMPS	VDDSMPS
		21	VDDSMPS	VLXSMPS
		23	VDD11	VSS
		24	VSS	V15SMPS
		46	VDD11	VSS
		47	VSS	V15SMPS
LQFP64 (10 x 10)	Compatible with differences on six pins related to internal SMPS power supply	28	VLXSMPS	VDDSMPS
		29	VDDSMPS	VLXSMPS
		31	VDD11	VSS
		32	VSS	V15SMPS
		62	VDD11	VSS
		63	VSS	V15SMPS
LQFP100 (14 x 14)	Compatible with differences on six pins related to internal SMPS power supply	46	VLXSMPS	VDDSMPS
		47	VDDSMPS	VLXSMPS
		49	VDD11	VSS
		50	VSS	V15SMPS
		98	VDD11	VSS
		99	VSS	V15SMPS
LQFP144 (20 x 20)	Compatible with differences on six pins related to internal SMPS power supply	68	VLXSMPS	VDDSMPS
		69	VDDSMPS	VLXSMPS
		71	VDD11	VSS
		72	VSS	V15SMPS
		142	VDD11	VSS
		143	VSS	V15SMPS
UFBGA132(7 x 7)	Compatible, but typical values of capacitors and coil are not the same Example with coils: 2.2 µH (STM32U5) versus 4.7 µH (STM32L5)	B4	VDD11 (2.2µF)	V15SMPS (4.7µF)
		M11	VDD11 (2.2µF)	V15SMPS (4.7µF)
UFBGA169 (7 x 7)	Not available for STM32L5, new STM32U575/585 specific ballout	-	-	-
WLCSP90 (4.1382 x 3.8952)		-	-	-

Note: The pattern of differences in the above tables is the same on all QFP packages. It is related to power supply pins.

Any adaptations between STM32L5 and STM32U575/585 packages support must be aware of the differences in capacitors and coil typical values connected to power supply pins.

3 Boot mode compatibility

3.1 Boot modes selection

For the STM32U575/585 and STM32L5, the BOOT0 input pin may come from the PH3-BOOT0 pin or from an option bit, depending on the value of a user option bit to free the GPIO pad if needed.

The bootloader is located in the system memory. It is used to reprogram the Flash memory by using USART, I2C, SPI, FDCAN or USB FS in device mode through the DFU (device firmware upgrade).

The STM32U575/585 and STM32L5 have compatible boot modes when TrustZone is disabled or enabled (see the tables below). Refer to the STM32U575/58 reference manual (RM0456) for more details.

Table 6. Boot modes when TrustZone is disabled (TZEN = 0)

nBOOT0 FLASH_ OPTR[27]	BOOT0 pin PH3	nSWBOOT0 FLASH_ OPTR[26]	Boot address option bytes selection	Boot area	ST programmed default value
-	0	1	NSBOOTADD0[24:0]	Boot address defined by user option bytes NSBOOTADD0[24:0]	Flash: 0x0800 0000
-	1	1	NSBOOTADD1[24:0]	Boot address defined by user option bytes NSBOOTADD1[24:0]	System bootloader: 0x0BF9 0000
1	-	0	NSBOOTADD0[24:0]	Boot address defined by user option bytes NSBOOTADD0[24:0]	Flash: 0x0800 0000
0	-	0	NSBOOTADD1[24:0]	Boot address defined by user option bytes NSBOOTADD1[24:0]	System bootloader: 0x0BF9 0000

Table 7. Boot modes when TrustZone is enabled (TZEN = 1)

BOOT _LOCK	nBOOT0 FLASH_ OPTR[27]	BOOT0 pin PH3	nSWBOOT0 FLASH_ OPTR[26]	RSS command	Boot address option-bytes selection	Boot area	ST programmed default value
0	-	0	1	0	SECBOOTADD0[24:0]	Secure boot address defined by user option bytes SECBOOTADD0[24:0]	Flash: 0x0C00 0000
	-	1	1	0	N/A	RSS: 0x0FF8 0000	
	1	-	0	0	SECBOOTADD0[24:0]	Secure boot address defined by user option bytes SECBOOTADD0[24:0]	Flash: 0x0C00 0000
	0	-	0	0	N/A	RSS: 0x0FF8 0000	
	-	-	-	≠0			
1	-	-	-	-	SECBOOTADD0[24:0]	Secure boot address defined by user option bytes SECBOOTADD0[24:0]	Flash: 0x0C00 0000

3.2 Embedded bootloader

The embedded bootloader is located in the system memory and programmed by ST during production. This bootloader allows the user to reprogram the Flash memory, using one of the serial interfaces listed in the table below.

Table 8. Bootloader interface on STM32L5 and STM32U575/585

Peripheral	Pin name (number)	STM32L5	STM32U575/585
DFU	USB_DM (PA11)	X	X
	USB_DP (PA12)	X	X
USART1	USART1_TX (PA9)	X	X
	USART1_RX (PA10)	X	X
USART2	USART2_TX (PA2)	X	X
	USART2_RX (PA3)	X	X
USART3	USART3_TX (PC10)	X	X
	USART3_RX (PC11)	X	X
I2C1	I2C1_SCL (PB6)	X	X
	I2C1_SDA (PB7)	X	X
I2C2	I2C2_SCL (PB10)	X	X
	I2C2_SDA (PB11)	X	X
I2C3	I2C3_SCL (PC0)	X	X
	I2C3_SDA (PC1)	X	X
I2C4	I2C4_SCL (PD12)	N/A	
	I2C4_SDA (PD13)		
SPI1	SPI1_NSS (PA4)	X	X
	SPI1_SCK (PA5)	X	X
	SPI1_MISO (PA6)	X	X
	SPI1_MOSI (PA7)	X	X
SPI2	SPI2_NSS (PB12)	X	X
	SPI2_SCK (PB13)	X	X
	SPI2_MISO (PB14)	X	X
	SPI2_MOSI (PB15)	X	X
SPI3	SPI3_NSS (PG12)	x	X
	SPI3_SCK (PG9)	x	X
	SPI3_MISO (PG10)	x	X
	SPI3_MOSI (PB5)	x	X
FDCAN1	CAN1_RX (PB8)	X	X
	CAN1_TX (PB9)	X	X

For more details on the bootloader, refer to the application note *STM32 microcontroller system memory boot mode* (AN2606).

4 Peripheral migration

4.1 STM32 products cross-compatibility

STM32 microcontrollers embed a set of peripherals that can be classified in the following groups:

- Group1: peripherals by definition common to all products

  Those peripherals are identical, so they have the same structure, registers and control bits. There is no need to perform any firmware change to keep the same functionality at the application level after migration. All the features and behavior remain the same.
- Group2: peripherals shared by all products but with only minor differences (in general to support new features)

  The migration from one product to another is very easy and does not need any significant new development effort.
- Group3: peripherals that have considerable changes from one product to another (new architecture or new features for example)

  For this group of peripherals, the migration requires a new development at application level.

The security architecture of STM32U575/585 and STM32L5 is based on Arm TrustZone with the Armv8-M mainline extension. Each GPIO or peripheral, DMA channel, clock configuration register, DCACHE1 (STM32U575/585 only), ICACHE or small part of Flash memory or SRAM, can be configured as trusted or untrusted.

Enhanced features of security are also implemented on STM32U575/585. Moreover, the STM32U575/585 and STM32L5 allow high performances and ultra-low power consumption features.

The STM32U575/585 innovative features include a best-in-class voltage regulator switching on-the-fly between DC/DC and LDO, according to the application requirements. The STM32U575/585 also include the new SRD (SmartRun domain) architecture that relies on a new low-power DMA (LPDMA1), allowing autonomous operation during low-power modes down to Stop 2. This architecture features internal SRAM (16-Kbyte SRAM4) and dedicated low-power peripherals.

The table below summarizes the available peripherals in STM32L5 and STM32U575/585 as well as their compatibility.

Table 9. STM32 peripheral compatibility between STM32L5 and STM32U575/585

Peripheral		STM32L5	STM32U575/585
Core		Cortex-M33	
Maximum CPU Frequency		110 MHz	160 MHz
Caches	ICACHE	1x ICACHE	
	DCACHE1	N/A	**DCACHE1 for external memories**
PWR/regulators	Power supply	1.71V to 3.6V	
	LDO	Available on all products	
	LDO + internal DC-DC	STM32L5xxxxxxQ products	STM32U5xxxxQ products **+ DC-DC/LDO on-the-fly selection** **Advanced features**
	LDO + external DC-DC	STM32L5xxxxxxP products	N/A (no regulator bypass option)
Flash memory	Size	512 Kbytes	2 Mbytes **Advanced features**
	Bank	Dual or single bank with TrustZone	Dual bank with TrustZone **Specific direct bus to Fast C-Bus**
SRAMs	SRAM1	192 Kbytes	

Peripheral		STM32L5	STM32U575/585
SRAMs	SRAM2	64 Kbytes	64 Kbytes with optional ECC
	SRAM3	N/A	**512 Kbytes** with optional ECC
	SRAM4		**16 Kbytes in SRD**
	Backup SRAM		**BKPSRAM (2 Kbytes)**
DMA (not compatible)		DMA1 and DMA2 (8 channels each)	GPDMA (16 channels) **Advanced Features**
		N/A	**LPDMA (4 channels) in SRD**
			DMA2D: Chrom-ART Accelerator
RCC		Up to 110 MHz	Up to 160 MHz **Registers not compatible** **More advanced features**
GTZC (global TrustZone controller)		STM32L5 features	STM32L5 features **+ Privilege mode extended to internal/external memories**
Anti-tamper detection		Eight tamper pins	
		128-byte backup registers	
		STM32L5 features	STM32L5 features **+ New advanced features**
CRC		1x CRC	
FSMC (external memory controller for static memory/LCD)		1x FSMC	
GPIOS		Up to 115	Up to 139 PB11 pin missing, replaced by VCAP
LPGPIOs		N/A	• **16 I/Os controlled by LPDMA down-to Stop 2 mode** • **LPGPIO designed to be used in conjunction with GPIO**
Timers	Advanced control	2 (16-bit)	
	General purpose	2 (32-bit) + 5 (16-bit)	4 (32-bit) + 3 (16-bit)
	Basic	2 (16-bit)	
	Low-power	3 (16-bit)	4 (16-bit) **Autonomous mode**
	Watchdogs	1x WWDG and 1x IWDG	1x WWDG and 1x IWDG **+ early interrupt feature**
	RTC	1x RTC	1x RTC **+ Binary mode selection**
	SysTick	1	
Communication interfaces	SPI	3x SPI	3x SPI **Advanced features** **Registers not compatible**
	I2C	4x I2C	4x I2C + **Autonomous mode**
	USART	3x USART	3x USART + **Autonomous mode**
	UART	2x UART	2x UART + **Autonomous mode**

Peripheral		STM32L5	STM32U575/585
Communication interfaces	LPUART	1x LPUART	1x LPUART + **Autonomous mode**
	SAI (audio interface)	2x SAI	
	FDCAN	1x FDCAN	
	USB	1x USB full-speed device	1x USB **OTG full-speed** device /**host/OTG** **NOT compatible with the STM32L5**
	UCPD	1x UCPD (USB Type C™ and Power Delivery interface)	
	SDMMC	1x SDMMC	**2x** SDMMC
	Camera interfaces	N/A	1x DCMI and **1x PSSI**
	OCTOSPI	1x OCTOSPI	2x OCTOSPI **+ I/O manager multiplexer**
Analog peripherals	ADC	2x 12-bit ADC (5 Msps)	1x 14-bit ADC (2.5 Msps) 1x 12-bit ADC (2.5 Msps) **+ New features** **+ Autonomous mode**
	DAC	1x 12-bit DAC	2x 12-bit DAC **Autonomous mode**
	COMP	2 comparators	2 comparators Registers not compatible
	OPAMP	2 operational amplifiers	2 operational amplifiers **New slew rate configuration**
	Voltage reference buffer	1x VREFBUF	
Cryptographic peripherals(1)	AES	1x AES	
	SAES (secure AES)	N/A	**1x SAES** **Secure AES** **Advanced features**
	OTFDEC (on-the-fly decryption)	1x OTFDEC On-the-fly decryption for OCTOSPI with same features	2x OTFDEC On-the-fly decryption for OCTOSPI with same features
	PKA (private key accelerator)	1x PKA	1x PKA **Advanced features**
	HASH (SHA-256)	1x HASH	
	RNG (true random number generator)	1x RNG	1x RNG **Transparent usage by SAES and PKA, for DPA resistance**
Signal-processing coprocessors accelerators	Digital filters	1x DFSDM, digital filters for sigma-delta modulators (four filters)	**1x MDF**, multi-function digital filter **(six filters)** **1x ADF**, audio digital filter **(one filter)** **Advanced features**
	CORDIC coprocessor	N/A	1x CORDIC
	FMAC (filter mathematical accelerator)		1x FMAC
	TSC (touch sensing controller)	24 channels	

1. *AES, OTFDEC and PKA only available on STM32L562xx and STM32U585xx devices. SAES only available on STM32U585xx devices.*

4.2 Secure and non-secure boundaries of peripheral memory mapping

The peripheral address mapping has been changed in the STM32U575/585 compared to the STM32L5.

The table below presents the peripherals register boundary addresses for STM32U575/585 compared to STM32L5. For more details on the memory mapping, refer to the product reference manual.

Table 10. STM32L5 and STM32U575/585 memory mapping for secure and non-secure boundary addresses

Peripheral (size in bytes)	STM32L5 bus	STM32L5		STM32U575/585 bus	STM32U575/585	
		Secure boundary address	Non-secure boundary address		Secure boundary address	Non-secure boundary address
LPDMA1 (4 K)	N/A			AHB3	0x5602 5000-0x5602 5FFF	0x4602 5000-0x4602 5FFF
ADF1 (4 K)					0x5602 4000-0x5602 4FFF	0x4602 4000-0x4602 4FFF
GTZC2_ MPCBB4 (1 K)					0x5602 3800-0x5602 3BFF	0x4602 3800-0x4602 3BFF
GTZC2_ TZIC (1 K)					0x5602 3400-0x5602 37FF	0x4602 3400-0x4602 37FF
GTZC2_ TZSC (1 K)					0x5602 3000-0x5602 33FF	0x4602 3000-0x4602 33FF
EXTI (1 K)	AHB1	0x5002 F400-0x5002 F7FF	0x4002 F400-0x4002 F7FF		0x5602 2000-0x5602 23FF	0x4602 2000-0x4602 23FF
DAC1 (1 K)	APB1	0x5000 7400-0x5000 77FF	0x4000 7400-0x4000 77FF		0x5602 1800-0x5602 1BFF	0x4602 1800-0x4602 1BFF
ADC2 or ADC4 (1 K) (For L5 and U5 respectively)	ADC2 shares the same interface with ADC1, functioning in interleaved mode				0x5602 1000-0x5602 13FF	0x4602 1000-0x4602 13FF
RCC (1 K)	AHB1	0X5002 1000-0x5002 13FF	0X4002 1000-0x4002 13FF		0x5602 0C00-0x5602 0FFF	0x4602 0C00-0x4602 0FFF
PWR (1 K)	APB1	0x5000 7000-0x5000 73FF	0x4000 7000-0x4000 73FF		0x5602 0800-0x5602 0BFF	0x4602 0800-0x4602 0BFF
LPGPIO (1 K)	N/A				0x5602 0000-0x5602 03FF	0x5602 0000-0x5602 03FF
TAMP (1 K)	APB1	0x5000 3400-0x5000 37FF	0x4000 3400-0x4000 37FF	APB3	0x5600 7C00-0x5600 7FFF	0x4600 7C00-0x4600 7FFF
RTC (1 K)		0x5000 2800-0x5000 2BFF	0x4000 2800-0x4000 2BFF		0x5600 7800-0x5600 7BFF	0x4600 7800-0x4600 7BFF
VREFBUF (1 K)	APB2	0x5001 0100-0x5001 01FF	0x4001 0100-0x4001 01FF		0x5600 7400-0x5600 77FF	0x4600 7400-0x4600 77FF
COMP (1 K)		0x5001 0200-0x5001 03FF	0x4001 0200-0x4001 03FF		0x5600 5400-0x5600 57FF	0x4600 5400-0x4600 57FF
OPAMP (1 K)	APB1	0x5000 7800-0x5000 7BFF	0x4000 7800-0x4000 7BFF		0x5600 5000-0x5600 53FF	0x4600 5000-0x4600 53FF
LPTIM4 (1 K)	N/A				0x5600 4C00-0x5600 4FFF	0x4600 4C00-0x4600 4FFF
LPTIM3 (1 K)	APB1	0x5000 9800-0x5000 9BFF	0x4000 9800-0x4000 9BFF		0x5600 4800-0x5600 4BFF	0x4600 4800-0x4600 4BFF

Peripheral (size in bytes)	STM32L5 bus	STM32L5		STM32U575/585 bus	STM32U575/585	
		Secure boundary address	Non-secure boundary address		Secure boundary address	Non-secure boundary address
LPTIM1 (1 K)	APB1	0x5000 7C00-0x5000 7FFF	0x4000 7C00-0x4000 7FFF	APB3	0x5600 4400-0x5600 47FF	0x4600 4400-0x4600 47FF
I2C3 (1 K)		0x5000 5C00-0x5000 5FFF	0x4000 5C00-0x4000 5FFF		0x5600 2800-0x5600 2BFF	0x4600 2800-0x4600 2BFF
LPUART1 (1 K)		0x5000 8000-0x5000 83FF	0x4000 8000-0x4000 83FF		0x5600 2400-0x5600 27FF	0x4600 2400-0x4600 27FF
SPI3 (1 K)		0x5000 3C00-0x5000 3FFF	0x4000 3C00-0x4000 3FFF		0x5600 2000-0x5600 23FF	0x4600 2000-0x4600 23FF
SYSCFG (1 K)	APB2	0x5001 0000-0x5001 002F	0x4001 0000-0x4001 002F		0x5600 0400-0x5600 07FF	0x4600 0400-0x4600 07FF
OCTOSPI2 registers (1 K)	N/A			AHB2	0x520D 2400-0x520D 27FF	0x420D 2400-0x420D 27FF
OCTOSPI1 registers (1 K)	AHB3	0x5402 1000-0x5402 13FF	0x4402 1000-0x4402 13FF		0x520D 1400-0x520D 17FF	0x420D 1400-0x420D 17FF
FSMC registers (1 K)		0x5402 0000-0x5402 03FF	0x4402 0000-0x4402 03FF		0x520D 0400-0x520D 07FF	0x420D 0400-0x420D 07FF
DLYBOS2 (1 K)[1]	N/A				0x520C F400-0x520C F7FF	0x420C F400-0x420C F7FF
DLYBOS1 (1 K)[1]					0x520C F000-0x520C F3FF	0x420C F000-0x420C F3FF
SDMMC2 (1 K)					0x520C 8C00-0x520C 8FFF	0x420C 8C00-0x420C 8FFF
DLYBSD2 (1 K)[1]					0x520C 8800-0x520C 8BFF	0x420C 8800-0x420C 8BFF
DLYBSD1 (1 K)[1]					0x520C 8400-0x520C 87FF	0x420C 8400-0x420C 87FF
SDMMC1 (1 K)	AHB2	0x520C 8000-0x520C 83FF	0x420C 8000-0x420C 83FF		0x520C 8000-0x520C 83FF	0x420C 8000-0x420C 83FF
OTFDEC2 (1 K)	N/A				0x520C 5400-0x520C 57FF	0x420C 5400-0x420C 57FF
OTFDEC1 (1 K)	AHB2	0x520C 5000-0x520C 53FF	0x420C 5000-0x420C 53FF		0x520C 5000-0x520C 53FF	0x420C 5000-0x420C 53FF
OCTOSPIM (1 K)	N/A				0x520C 4000-0x520C 43FF	0x420C 4000-0x420C 43FF
PKA (8 K)	AHB2	0x520C 2000-0x520C 3FFF	0x420C 2000-0x420C 3FFF		0x520C 2000-0x520C 3FFF	0x420C 2000-0x420C 3FFF
SAES (1 K)	N/A				0x520C 0C00-0x520C 0FFF	0x420C 0C00-0x420C 0FFF
RNG (1 K)	AHB2	0x520C 0800-0x520C 0BFF	0x420C 0800-0x420C 0BFF		0x520C 0800-0x520C 0BFF	0x420C 0800-0x420C 0BFF
HASH (1 K)		0x520C 0400-0x520C 07FF	0x420C 0400-0x420C 07FF		0x520C 0400-0x520C 07FF	0x420C 0400-0x420C 07FF
AES (1 K)		0x520C 0000-0x520C 03FF	0x420C 0000-0x420C 03FF		0x520C 0000-0x520C 03FF	0x420C 0000-0x420C 03FF
OTG_FS (544 K)	The STM32L5 embed the USB OTG peripheral.				0x5203 8000-0x520B FFFF	0x4203 8000-0x420B FFFF
PSSI (1 K)	N/A				0x5202 C400-0x5202 C7FF	0x4202 C400-0x4202 C7FF

Peripheral (size in bytes)	STM32L5 bus	STM32L5		STM32U575/585 bus	STM32U575/585	
		Secure boundary address	Non-secure boundary address		Secure boundary address	Non-secure boundary address
DCMI (1 K)	N/A			AHB2	0x5202 C000-0x5202 C3FF	0x4202 C000-0x4202 C3FF
ADC1 (1 K)	AHB2	0x5202 8000-0x5202 83FF	0x4202 8000-0x4202 83FF		0x5202 8000-0x5202 83FF	0x4202 8000-0x4202 83FF
GPIOI (1 K)	N/A				0x5202 2000-0x5202 23FF	0x4202 2000-0x4202 23FF
GPIOH (1 K)	AHB2	0x5202 1C00-0x5202 1FFF	0x4202 1C00-0x4202 1FFF		0x5202 1C00-0x5202 1FFF	0x4202 1C00-0x4202 1FFF
GPIOG (1 K)		0x5202 1800-0x5202 1BFF	0x4202 1800-0x4202 1BFF		0x5202 1800-0x5202 1BFF	0x4202 1800-0x4202 1BFF
GPIOF (1 K)		0x5202 1400-0x5202 17FF	0x4202 1400-0x4202 17FF		0x5202 1400-0x5202 17FF	0x4202 1400-0x4202 17FF
GPIOE (1 K)		0x5202 1000-0x5202 13FF	0x4202 1000-0x4202 13FF		0x5202 1000-0x5202 13FF	0x4202 1000-0x4202 13FF
GPIOD (1 K)		0x5202 0C00-0x5202 0FFF	0x4202 0C00-0x4202 0FFF		0x5202 0C00-0x5202 0FFF	0x4202 0C00-0x4202 0FFF
GPIOC (1 K)		0x5202 0800-0x5202 0BFF	0x4202 0800-0x4202 0BFF		0x5202 0800-0x5202 0BFF	0x4202 0800-0x4202 0BFF
GPIOB (1 K)		0x5202 0400-0x5202 07FF	0x4202 0400-0x4202 07FF		0x5202 0400-0x5202 07FF	0x4202 0400-0x4202 07FF
GPIOA (1 K)		0x5202 0000-0x5202 03FF	0x4202 0000-0x4202 03FF		0x5202 0000-0x5202 03FF	0x4202 0000-0x4202 03FF
BKPSRAM (2 K)	N/A (only registers)			AHB1	0x5003 6400-0x5003 6BFF	0x4003 6400-0x4003 6BFF
GTZC1_ MPCBB3 (1 K)					0x5003 3400-0x5003 37FF	0x4003 3400-0x4003 37FF
GTZC1_ MPCBB2 (1 K)	AHB1	0x5003 3000-0x5003 33FF	0x4003 3000-0x4003 33FF		0x5003 3000-0x5003 33FF	0x4003 3000-0x4003 33FF
GTZC1_ MPCBB1 (1 K)		0x5003 2C00-0x5003 2FFF	0x4003 2C00-0x4003 2FFF		0x5003 2C00-0x5003 2FFF	0x4003 2C00-0x4003 2FFF
GTZC1_ TZIC (1 K)		0x5003 2800-0x5003 2BFF	0x4003 2800-0x4003 2BFF		0x5003 2800-0x5003 2BFF	0x4003 2800-0x4003 2BFF
GTZC1_ TZSC (1 K)		0x5003 2400-0x5003 27FF	0x4003 2400-0 x4003 27FF		0x5003 2400-0x5003 27FF	0x4003 2400-0x4003 27FF
DCACHE1 (1 K)	N/A				0x5003 1400 - 0x5003 17FF	0x4003 1400 - 0x4003 17FF
ICACHE (1 K)	AHB1	0x5003 0400-0x5003 07FF	0x4003 0400-0x4003 07FF		0x5003 0400-0x5003 07FF	0x4003 0400-0x4003 07FF
DMA2D (3 K)	N/A (only registers)				0x5002 B000-0x5002 BBFF	0x4002 B000-0x4002 BBFF
RAMCFG (4 K)					0x5002 6000-0x5002 6FFF	0x4002 6000-0x4002 6FFF
MDF1 (4 K)					0x5002 5000-0x5002 5FFF	0x4002 5000-0x4002 5FFF
TSC (1 K)	AHB1	0x5002 4000-0x5002 43FF	0x4002 4000-0x4002 43FF		0x5002 4000-0x5002 43FF	0x4002 4000-0x4002 43FF
CRC (1 K)		0x5002 3000-0x5002 33FF	0x4002 3000-0x4002 33FF		0x5002 3000-0x5002 33FF	0x4002 3000-0x4002 33FF

Peripheral (size in bytes)	STM32L5 bus	STM32L5		STM32U575/585 bus	STM32U575/585	
		Secure boundary address	Non-secure boundary address		Secure boundary address	Non-secure boundary address
FLASH registers (1 K)	AHB1	0x5002 2000-0x5002 23FF	0x4002 2000-0x4002 23FF	AHB1	0x5002 2000-0x5002 23FF	0x4002 2000-0x4002 23FF
FMAC (1 K)	N/A				0X5002 1400-0x5002 17FF	0X4002 1400-0x4002 17FF
CORDIC (1 K)					0X5002 1000-0x5002 13FF	0X4002 1000-0x4002 13FF
GPDMA1 (4 K)	DMAMUX1, DMA2 and DMA1 are present in STM32L5 with different features.				0x5002 0000-0x5002 0FFF	0x4002 0000-0x4002 0FFF
SAI2 (1 K)	APB2	0x5001 5800-0x5001 5BFF	0x4001 5800-0x4001 5BFF	APB2	0x5001 5800-0x5001 5BFF	0x4001 5800-0x4001 5BFF
SAI1 (1 K)		0x5001 5400-0x5001 57FF	0x4001 5400-0x4001 57FF		0x5001 5400-0x5001 57FF	0x4001 5400-0x4001 57FF
TIM17 (1 K)		0x5001 4800-0x5001 4BFF	0x4001 4800-0x4001 4BFF		0x5001 4800-0x5001 4BFF	0x4001 4800-0x4001 4BFF
TIM16 (1 K)		0x5001 4400-0x5001 47FF	0x4001 4400-0x4001 47FF		0x5001 4400-0x5001 47FF	0x4001 4400-0x4001 47FF
TIM15 (1 K)		0x5001 4000-0x5001 43FF	0x4001 4000-0x4001 43FF		0x5001 4000-0x5001 43FF	0x4001 4000-0x4001 43FF
USART1 (1 K)		0x5001 3800-0x5001 3BFF	0x4001 3800-0x4001 3BFF		0x5001 3800-0x5001 3BFF	0x4001 3800-0x4001 3BFF
TIM8 (1 K)		0x5001 3400-0x5001 37FF	0x4001 3400-0x4001 37FF		0x5001 3400-0x5001 37FF	0x4001 3400-0x4001 37FF
SPI1 (1K)		0x5001 3000-0x5001 33FF	0x4001 3000-0x4001 33FF		0x5001 3000-0x5001 33FF	0x4001 3000-0x4001 33FF
TIM1 (1 K)		0x5001 2C00-0x5001 2FFF	0x4001 2C00-0x4001 2FFF		0x5001 2C00-0x5001 2FFF	0x4001 2C00-0x4001 2FFF
UCPD1 (1 K)	APB1	0x5000 DC00-0x5000 DFFF	0x4000 DC00-0x4000 DFFF	APB1	0x5000 DC00-0x5000 DFFF	0x4000 DC00-0x4000 DFFF
FDCAN1 RAM (1 K)		0x5000 AC00-0x5000 AFFF	0x4000 AC00-0x4000 AFFF		0x5000 AC00-0x5000 AFFF	0x4000 AC00-0x4000 AFFF
FDCAN1 (1 K)		0x5000 A400-0x5000 A7FF	0x4000 A400-0x4000 A7FF		0x5000 A400-0x5000 A7FF	0x4000 A400-0x4000 A7FF
LPTIM2 (1 K)		0x5000 9400-0x5000 97FF	0x4000 9400-0x4000 97FF		0x5000 9400-0x5000 97FF	0x4000 9400-0x4000 97FF
I2C4 (1K)		0x5000 8400-0x5000 87FF	0x4000 8400-0x4000 87FF		0x5000 8400-0x5000 87FF	0x4000 8400-0x4000 87FF
CRS (1 K)		0x5000 6000-0x5000 63FF	0x4000 6000-0x4000 63FF		0x5000 6000-0x5000 63FF	0x4000 6000-0x4000 63FF
I2C2 (1 K)		0x5000 5800-0x5000 5BFF	0x4000 5800-0x4000 5BFF		0x5000 5800-0x5000 5BFF	0x4000 5800-0x4000 5BFF
I2C1 (1 K)		0x5000 5400-0x5000 57FF	0x4000 5400-0x4000 57FF		0x5000 5400-0x5000 57FF	0x4000 5400-0x4000 57FF
UART5 (1 K)		0x5000 5000-0x5000 53FF	0x4000 5000-0x4000 53FF		0x5000 5000-0x5000 53FF	0x4000 5000-0x4000 53FF
UART4 (1 K)		0x5000 4C00-0x5000 4FFF	0x4000 4C00-0x4000 4FFF		0x5000 4C00-0x5000 4FFF	0x4000 4C00-0x4000 4FFF
USART3 (1 K)		0x5000 4800-0x5000 4BFF	0x4000 4800-0x4000 4BFF		0x5000 4800-0x5000 4BFF	0x4000 4800-0x4000 4BFF

Peripheral (size in bytes)	STM32L5 bus	STM32L5		STM32U575/585 bus	STM32U575/585	
		Secure boundary address	Non-secure boundary address		Secure boundary address	Non-secure boundary address
USART2 (1 K)	APB1	0x5000 4400-0x5000 47FF	0x4000 4400-0x4000 47FF	APB1	0x5000 4400-0x5000 47FF	0x4000 4400-0x4000 47FF
SPI2 (1 K)		0x5000 3800-0x5000 3BFF	0x4000 3800-0x4000 3BFF		0x5000 3800-0x5000 3BFF	0x4000 3800-0x4000 3BFF
IWDG (1 K)		0x5000 3000-0x5000 33FF	0x4000 3000-0x4000 33FF		0x5000 3000-0x5000 33FF	0x4000 3000-0x4000 33FF
WWDG (1 K)		0x5000 2C00-0x5000 2FFF	0x4000 2C00-0x4000 2FFF		0x5000 2C00-0x5000 2FFF	0x4000 2C00-0x4000 2FFF
TIM7 (1 K)		0x5000 1400-0x5000 17FF	0x4000 1400-0x4000 17FF		0x5000 1400-0x5000 17FF	0x4000 1400-0x4000 17FF
TIM6 (1 K)		0x5000 1000-0x5000 13FF	0x4000 1000-0x4000 13FF		0x5000 1000-0x5000 13FF	0x4000 1000-0x4000 13FF
TIM5 (1 K)		0x5000 0C00-0x5000 0FFF	0x4000 0C00-0x4000 0FFF		0x5000 0C00-0x5000 0FFF	0x4000 0C00-0x4000 0FFF
TIM4 (1 K)		0x5000 0800-0x5000 0BFF	0x4000 0800-0x4000 0BFF		0x5000 0800-0x5000 0BFF	0x4000 0800-0x4000 0BFF
TIM3 (1 K)		0x5000 0400-0x5000 07FF	0x4000 0400-0x4000 07FF		0x5000 0400-0x5000 07FF	0x4000 0400-0x4000 07FF
TIM2 (1 K)		0x5000 0000-0x5000 03FF	0x4000 0000-0x4000 03FF		0x5000 0000-0x5000 03FF	0x4000 0000-0x4000 03FF

1. *Belongs to DLYB (delay block) peripheral that is used to generate an output clock de-phased from the input clock. Delays are needed by OCTOSPIx and SDMMCx peripherals.*

5 Migration of security peripherals

5.1 TAMP

The STM32U575/585 anti-tamper detection circuit is used to protect sensitive data from external attacks. 32 backup registers, each of 32-bit size, are retained in all low-power modes and also in VBAT mode. The main differences between STM32U575/585 and STM32L5 are detailed below.

5.1.1 Tamper pins and internal events

The table below compares the tamper pins and internal events and lists the main differences between STM32U575/585 and STM32L5.

Table 11. Tamper pins and events for STM32L5 and STM32U575/585

Feature	STM32L5	STM32U575/585
Tamper pins (not compatible)	8 input/output TAMP pins for 8 external tamper detection events	
	PE6 (TAMP_IN3/TAMP_OUT6) PC13 (TAMP_IN1/TAMP_OUT2) PA0 (TAMP_IN2/TAMP_OUT1) PA1 (TAMP_IN5/TAMP_OUT4) PC5 (TAMP_IN4/TAMP_OUT5)	
	PF7 (TAMP_IN6/TAMP_OUT3)	PE3 (TAMP_IN6/TAMP_OUT3)
	PF8 (TAMP_IN7/TAMP_OUT8)	PE4 (TAMP_IN7/TAMP_OUT8)
	PF9 (TAMP_IN8/TAMP_OUT7)	PE5 (TAMP_IN8/TAMP_OUT7)
TAMP internal events to protect against transient or environmental perturbation attacks (four new internal tampers in STM32U575/585)	5 internal tamper events	11 internal tamper events
	• *tamp_itamp1*: Supply voltage monitoring • *tamp_itamp2*: Temperature monitoring • *tamp_itamp3*: LSE monitoring • *tamp_itamp5*: RTC calendar overflow • *tamp_itamp8*: Monotonic counter overflow	
	N/A	• *tamp_itamp6*: JTAG/SWD access when RDP > 0 • *tamp_itamp7*: Voltage monitoring through ADC analog watchdog 1 • *tamp_itamp9*: Cryptographic peripheral fault (SAES, AES, PKA or TRNG) • *tamp_itamp11*: IDWG reset when tamper flag is set • *tamp_itamp12*: Voltage monitoring through ADC analog watchdog 2 • *tamp_itamp13*: Voltage monitoring through ADC analog watchdog 3
List of device **secrets erased** by tamper	• Backup registers • SRAM2 • PKA SRAM	
	ICACHE	ICACHE/DCACHE1
	N/A	• Backup SRAM (optionally) • OTFDEC keys and CRC registers • SAES, AES, HASH peripherals

Feature	STM32L5	STM32U575/585
Tamper software filtering (**potential tamper**)	Configuration to detect tamper events without erasing secrets (NOERASE mode)	NOERASE mode **with access to device secrets blocked**
	Software control to launch device secrets erase	Software control to launch device secrets erase **+ timeout**
TAMP pins functionality over **V_{DD} mode**	All tamper pins, TAMP_IN[8:1] and TAMP_OUT[8:1], are functional in all low-power modes when external V_{DD} power supply is present.	
TAMP pins functionality over **V_{BAT} mode**	Only TAMP_IN1, TAMP_IN 2 and TAMP_IN 3 are functional in VBAT mode. Only TAMP_OUT2 is functional in V_{BAT} mode.	All tamper pins, TAMP_IN[8:1] and TAMP_OUT[8:1], are functional in V_{BAT} mode.
LSE monitoring (*tamp_itamp3*) See section 'Clock security system on LSE' in the product reference manual for more details)	LSE missing detection	
	N/A	LSE over-frequency detection LSE under-frequency
	CSS on LSE works in all modes **except V_{BAT}**.	CSS on LSE works in all modes **including V_{BAT}**.
	LSE clock is no longer supplied to the RTC.	LSE clock is no longer supplied to the RTC.
Temperature monitoring (*tamp_itamp2*)	Not functional in V_{BAT} mode	Functional in V_{BAT} mode
	A tamper event is generated when the temperature is above or below the functional range.	
Voltage Supply monitoring (*tamp_itamp1*) See section 'Backup domain voltage and temperature monitoring' in the product reference manual.	The monitoring is performed on V_{DD}.	The monitoring is performed on Backup domain supply that is V_{DD} when present, V_{BAT} otherwise.
	Not functional in V_{BAT} mode	Functional in V_{BAT} mode
	A tamper event (*tamp_itamp1*) is generated when V_{DD} is above the specified threshold.	A tamper event (*tamp_itamp1*) is generated when the Backup domain voltage is above the specified thresholds.
	A BOR (Brownout reset) is generated when V_{DD} is below the functional range.	A Backup domain BOR is generated when V_{BAT} voltage is below the functional range, in VBAT mode.
	N/A	In case of Backup domain BOR, all the device is erased including the Backup domain.

5.1.2 Potential tamper detection mode (STM32U575/585 only)

In the NOERASE configuration (see section 'TAMP backup registers and other device secrets erase' in the reference manual (RM0456) for more details), the backup registers and other device secrets are not reset when the corresponding tamper event is detected. In addition, the read and write accesses to the backup registers and to other device secrets are blocked.

The *tamp_potential* signal is used to block the read and write accesses to the following device secrets:

- backup registers
- backup SRAM (optionally)
- SRAM2
- HWKEY in system Flash memory

In this case, the software can launch secrets erase when the potential tamper is confirmed to be a true one. The *tamp_potential* signal is used to erase the device secrets listed hereafter and the device secrets access is blocked when erase is on-going:

- ICACHE content
- SAES, AES, HASH peripherals
- PKA SRAM

The backup registers and other device secrets are reset by software by setting the BKERASE bit in the TAMP_CR2 register. The internal tamper 11 generates a tamper event if the independent watchdog reset occurs when a tamper flag is set. This forces by hardware the reset of the backup registers and other device secrets after a timeout, in case the tamper source is in NOERASE configuration.

5.1.3 Boot master key

The first eight backup registers can be used to store a boot master key, programmed during boot for the SAES (secure AES). Once locked, the eight backup registers cannot be accessed anymore by software: they are read as 0 and write to these registers is ignored.

The locking bit SMKLOCK cannot be cleared by software. It is cleared either by hardware following a tamper event or when the readout protection (RDP) is disabled. In both cases, the backup registers are also erased. Refer to section 'Boot hardware key' of the reference manual (RM0456) for more details.

5.2 HASH (hash processor)

The STM32U575/585 and STM32L5 embed a HASH hardware accelerator with same features. Both hash processors provide an interface to connect to the DMA controller. The STM32U575/585 HASH peripheral supports both single and fixed DMA burst transfers of four words. However, the STM32L5 HASH only supports single DMA transfers.

The HASH registers are compatible, except a minor difference between STM32U575/585 and STM32L5 HASH_CR registers (ALGO[0] is moved from bit 7 to bit 17).

5.3 OTFDEC (on-the-fly decryption engine)

The STM32U585 embed two OTFDEC peripherals versus only one in STM32L562 with the same features.

The OTFDEC decrypts in real-time the encrypted content stored in the external OCTOSPI memories used in Memory-mapped mode. The OTFDEC uses the AES-128 algorithm in counter mode (CTR).

5.4 RNG (true random number generator)

The STM32U575/585 and STM32L5 embed a TRNG that delivers 32-bit random numbers generated by an integrated analog circuit. The latter provides full entropy raw data composed of a live entropy source (analog) and an internal conditioning component.

The RNG is a NIST SP 800-90B compliant entropy source that can be used to construct a non-deterministic random bit generator (NDRBG). It has also been tested using German BSI statistical tests of AIS-31 (T0 to T8).

STM32U575/585 and STM32L5 RNG peripherals have the same features with minor new ones added to the STM32U575/585, as shown in the table below.

Table 12. RNG features on STM32L5 and STM32U575/585

RNG features	STM32L5	STM32U575/585
True random number generator	X	X
Can be used as entropy source to construct a non-deterministic random bit generator (NDRBG)	X	X
NIST SP800-90B approved	X	X
Tested using German BSI statistical tests of AIS-31 (T0 to T8)	X	X
Embeds start-up and NIST SP800-90B approved continuous health tests	X	X
Can be disabled to reduce power consumption Enabled with an automatic low power mode (default configuration).	X	X
AHB slave peripheral, accessible through 32-bit word single accesses only	X	X
RNG internal tamper event signal to TAMP	N/A	X
Transparent use by SAES and PKA for DPA resistance	N/A	X

The RNG is transparently used by SAES and PKA for DPA resistance. When an unexpected error is found by the RNG, an internal tamper event is triggered in TAMP peripheral, and the RNG stops delivering random data.

When this event occurs, a secure application needs to reset the RNG either using the central reset management or the global SoC reset. Then a proper initialization of the RNG is required, again.

5.5 PKA (public key accelerator)

The STM32U585 and STM32L562 embed one PKA peripheral intended for the computation of cryptographic public key primitives within the Montgomery domain. All needed computations are performed within the accelerator, so no further hardware/software elaboration is needed to process the inputs or the outputs.

The STM32U585 and STM32L562 share almost the same PKA features but the STM32U585 embed two new features and three new computation operators. Registers are compatible except new bits added in STM32U585 to map the new features.

Table 13. PKA features for STM32L562 and STM32U585

Feature/operation	STM32L562	STM32U585
RSA modular exponentiation, RSA Chinese remainder theorem (CRT) exponentiation	X	X
ECC scalar multiplication, point on curve check	X	X
ECC complete addition	N/A	X
ECC double base ladder	N/A	X
ECC projective to affine	N/A	X
ECDSA signature generation and verification	X	X
Size of RSA/DH operands (in bits)	3136	4160
Size of ECC operands (in bits)	640	
Arithmetic and modular operations such as addition, subtraction, multiplication, modular reduction, modular inversion, comparison, and Montgomery multiplication	X	X
Built-in Montgomery domain inward and outward transformations	X	X
Protection against differential power analysis (DPA) and related side-channel attacks	N/A	X

5.6 AES and SAES hardware accelerators

The STM32U585 embed two AES accelerators: one secure AES (SAES) and a faster AES. The STM32L562 embed only one fast AES that shares the same features as the AES embedded in the STM32U585.

In STM32U585, the SAES with hardware unique key embeds protection against differential power analysis (DPA) and related side channel attacks. When an unexpected hardware fault occurs, an output tamper event is triggered and the AES automatically clears key registers. A reset is required for the AES to be usable again.

In STM32U585, the SAES has secure bus interfacing the true RNG that seeds the embedded PRNG module within SAES. The latter ensures cryptographically separated secure storage keys management (secure, privileged) and a key usage enforcement shared with the AES.

The AES can use the SAES as security coprocessor. In this case, secure application prepares the key in robust SAES, then, when ready, the AES can load this key through a dedicated hardware keybus. Recommended sequences are described in sections 'AES shared key usage' and 'SAES operations with shared keys' of the reference manual (RM0456).

The table below gives the main differences between STM32U585 and STM32L562 AES peripherals. The other features are the same, as described in the product reference manuals.

Table 14. AES/SAES features on STM32U585 and STM32L562

Modes and features	STM32L562	STM32U585	
	AES	AES	SAES
ECB, CBC chaining	X	X	X
CTR, CCM, GCM chaining	X	X	-
AES 128-bit ECB encryption (in cycles)	51	51	528
256-bit software key	X	X	X
DHUK and BHK key selection	-	-	X
Protection against DPA and related side-channel attacks	-	-	X
Shared key between SAES and AES	-	X	
AES tamper signal triggering	-	X	
AES interrupts and error managements	Computation completed flag and read/write error flag		
	-	Key error flag	
	-	-	RNG error flag
Registers compatibility	Registers compatible except new registers and bits added in STM32U575/585 to map the new features		

5.7 GTZC (global TrustZone controller)

The security architecture of STM32U575/585 and STM32L5 is based on Arm TrustZone with the Armv8-M mainline extension. Each GPIO or peripheral, DMA channel, clock configuration register, DCACHE/ICACHE or small part of Flash memory or SRAM can be configured as trusted or untrusted.

The GTZC embedded in the STM32U575/585 is used to configure secure-TrustZone and privileged attributes within the full system. It contains the following sub-blocks:

- TZSC: TrustZone security controller

  This sub-block defines the secure/privileged state of slave peripherals. It also controls the sub-region area size and properties for the watermark memory peripheral controller (MPCWM). The TZSC informs some peripherals (such as RCC or GPIOs) about the secure status of each securable peripheral, by sharing with RCC and I/O logic.
- MPCBB: memory protection controller - block based

  This sub-block configures the internal RAM in a TrustZone-system product having segmented SRAM (pages of 512 bytes) with programmable-security and privileged attributes.
- TZIC: TrustZone illegal access controller

  This sub-block gathers all illegal access events in the system and generates a secure interrupt towards NVIC.

The STM32U575/585 and STM32L5 GTZC registers are different (see the table below).

Table 15. GTZC features in STM32L5 and STM32U575/585

Features	STM32L5	STM32U575/585
Three independent 32-bit AHB interfaces for TZSC, TZIC and MPCBB	X	X
TZIC accessible only with secure transactions	X	X
Secure and non-secure access supported for privileged and unprivileged part of TZSC	X	X
Secure and non-secure access supported for privileged and unprivileged part of MPCBB	N/A (secure/non-secure only)	X
Registers to define secure blocks for internal and external SRAMs	X	X
Registers to define privileged blocks for internal and external SRAMs	N/A	X
Secure/privileged regions for internal backup SRAM	N/A	X
Secure/privileged access mode for securable and TrustZone-aware peripherals	X	X
Secure/privileged access mode for securable masters	X	X

5.7.1 GTZC implementation and resource assignments

The STM32U575/585 embed two instances of GTZC versus only one instance in STM32L5 (see the table below).

Table 16. GTZC implementation in STM32L5 and STM32U575/585

Feature	STM32L5	STM32U575/585	
GTZC block implemented	GTZC	GTZC1	GTZC2
Number of TZSC	1	1	1
Number of TZIC	1	1	1
Number of MPCBB	2	3	1
Number of MPCWM	3	5	N/A

MPCWM and MPCBB resources assignments are detailed in the tables below.

Table 17. MPCWM resources in STM32L5 and STM32U575/585

Product	GTZC block	MPC	Target memory interface	Number of secure/ non-secure and privileged/ unprivileged regions	Watermark granularity (bytes)
STM32U575/585	GTZC1	MPCWM1	OCTOSPI1	2	128 K
		MPCWM2	FSMC_NOR bank	2	128 K
		MPCWM3	FSMC_NAND bank	1	128 K
		MPCWM4	BKPSRAM	1	32
		MPCWM5	OCTOSPI2	2	128 K
STM32L5	GTZC	MPCWM1	OCTOSPI	2	128 K
		MPCWM2	FMC_NOR bank	2	
		MPCWM3	FMC_NAND bank	1	

Table 18. **MPCBB resources in STM32L5 and STM32U575/585**

Product	GTZC block	MPC	Resource	Memory size (Kbytes)	Block size (bytes)	Number of blocks	Number of super-blocks
STM32U575/585	GTZC1	MPCBB1	SRAM1	192	512	384	12
		MPCBB2	SRAM2	64		128	4
		MPCBB3	SRAM3	512		1024	32
	GTZC2	MPCBB4	SRAM4	16		32	1
STM32L5	GTZC	MPCBB1	SRAM1	192	256	768	24
		MPCBB2	SRAM2	64		256	8

5.7.2 TrustZone security architecture

When the TrustZone is enabled, the Armv8-M attributes define the access permissions based on secure and non-secure state:

- SAU (security attribution unit): up to eight SAU configurable regions available for security attribution
- IDAU (implementation defined attribution unit): provides a first memory partition as non-secure or non-secure callable attributes. This partition is then combined with the results from the SAU security attribution and the higher-security state is selected.

Based on IDAU security attribution, the Flash memory, system SRAMs and peripheral memory space are aliased twice for secure and non-secure states. However, the external memory space is not aliased.

The STM32U575/585 and STM32L5 datasheets give the same example of memory map security attribution versus SAU configuration regions.

5.7.3 TrustZone peripheral classification

When the TrustZone security is active, a peripheral can be either securable or TrustZone-aware as follows:

- securable: peripheral protected by an AHB/APB firewall gate that is controlled from TZSC to define security properties
- TrustZone-aware: peripheral connected directly to AHB or APB bus and implementing a specific TrustZone behavior such as a subset of registers being secure

The default system security state is the same for STM32L5 and STM32U575/585.

6 Migration of system peripherals

This section analyzes the differences and similarities between system peripherals implemented in STM32L5 and STM32U575/585.

6.1 SYSCFG (system configuration controller)

The table below shows the differences between the SYSCFG in STM32L5 and in STM32U575/585.

Table 19. SYSCFG features in STM32L5 and STM32U575/585

Features	STM32L5	STM32U575/585
Common features	Managing robustness feature	
	Configuring TrustZone security register access	
	Configuring FPU interrupts	
	Driving capability on some I/Os and voltage booster for I/Os analog switches	
Managing I/O compensation cells	N/A	Compensation cells on V_{DD}/V_{DDIO2} track the PVT conditions to control the current slew-rate and output impedance in I/O buffer.
SRAM2 WRP	Setting SRMA2 write protection and software erase	N/A (performed by the RAMCFG)
UCPD filter enable	N/A (only UCPD features available without filter)	UCPD BMC receiver low-pass analog filter enable (as defined by tRxFilter in the standard)
I^2C Fast-mode Plus	Enabling/disabling the I^2C I/Os Fast-mode Plus drive	I^2C I/Os Fast-mode Plus drive is controlled from the I2C peripheral. This mode can still be enabled/disabled in SYSCFG for four I/Os when not used by I2C.

6.2 Flash memory

Compared to the STM32L5, the STM32U575/585 Flash memory includes bigger memory space with advanced features (see the table below).

Table 20. Flash memory features in STM32L5 and STM32U575/585

Feature	STM32L5	STM32U575/585
Size	512 Kbytes (128 x 2-Kbyte pages): • Single-bank page size is 4 Kbytes. • Dual bank page size is 2 Kbytes.	2-Mbyte dual bank (128 x 8-Kbyte pages)
	Non-secure information block: • System memory: 32 Kbytes • OTP area: 512 bytes	
	Secure information block: • RSS: 8 Kbytes • RSS library: 2 Kbytes	Secure information block • RSS: 24 Kbytes • RSS library: 8 Kbytes
Access modes	Read (R), write (W) and read-wile-write (RWW)	
	Single bank mode (DBANK = 0): 128-bit read access Dual bank mode (DBANK = 1): 64-bit read access	Dual bank mode: 128-bit read access (no single bank mode)

Feature	STM32L5	STM32U575/585
ECC	8 bits per 64-bit double word (SECDED). The ECC mechanism supports: • one error detection and correction • two errors detection	9 bits per 128-bit quad word (SECDED). The ECC mechanism supports: • one error detection and correction • two errors detection
Read-access latency	Up to 4 wait-states (WS) depending on the supply voltage and the frequency	The Flash memory supports a low-power read mode (LPM). The number of WS depends on LPM: • LPM = 0: up to 4 WS depending on supply voltage and frequency • LPM = 1 (reduced consumption and increased latency): up to 15 WS depending on supply voltage and frequency
	Increasing/decreasing the CPU frequency to tune the number of wait statements.	
	N/A	Instruction prefetch through ICACHE can be enabled by setting the PRFTEN bit that increases code execution. Programmable switching sequences between normal read mode to low-power mode (and vice-versa).
Power-down mode per Bank	N/A	After reset, both banks are in normal mode. Each bank can be independently put in power-down mode.
New endurance capability	10 kcycles	Increased endurance thanks to the smart write module: • 10 kcycles (written and erased) on 2 Mbytes • 100 kcycles(written and erased) on 256 Kbytes per bank
Flash program and erase operations	Page/bank if dual bank activated/mass erase	Page/bank/mass erase
	64-bit (double word) programming	128-bit (quad word) programming
New option bytes	N/A	8 additional option bytes versus STM32L5 (see Table 21): • IO_VDDIO2_HSLV/IO_VDD_HSLV • SRAM134_RST • OEM1KEY/OEM2KEY (4 option bytes) • UNLOCK write protections (4 options bits)
Flash memory protection	Write protection (WRP)	
	Readout protection (RDP)	
	Secure protection when TrustZone is active: • up to 2 secure watermark-based non-volatile areas • up to 2 secure block-based volatile areas • up to 2 secure-hide protection areas	Additional secure protection when TrustZone is active: • up to 2 secure watermark-based non-volatile areas • secure block-based volatile areas with page granularity • up to 2 secure hide-protection areas
	Privilege protection bit (PRIV) for both privileged or unprivileged, secure and non-secure access	Privileged block-based volatile areas with page granularity. PRIV bit in STM32L5 is replaced by SPRIV and NSPRIV in STM32U575/585. • Any page programmable on-the-fly as privileged or unprivileged • Privilege register protection: Grant Flash register access to privilege code independently for secure (SPRIV) and non-secure (NSPRIV) accesses

Feature	STM32L5	STM32U575/585
Locking keys for RDP regression from L1 and L2	The RDP transition between levels is performed by modifying the option bytes values: • full mass erase performed only when L1 or L0.5 is active and L0 is requested • no mass erase when the protection level is increased (such as 0 to 0.5 or 1 to 2)	
	No OEM locking key between levels Regression not allowed between L2 and L1	OEM key required in RDP transition between levels: • possible RDP transition between L1 and L0 with OEM1 key • possible RDP transition between L2 and L1 with OM2 key • possible RDP transition between L1 and L0.5 with OEM2 key
	Regression possible from L0.5 or L1 to L0, and L1 to L0.5. Regression not possible from L2.	Regression not possible from L0.5. Regression possible from L2 with OEM2Keys when provisioned. Regression always possible from L1. OEM1Key are mandatory from L1 to L0 when provisioned.

The option bytes are configured by the end user depending on the application requirements (see the table below and refer to section 'Flash memory option bytes' of the product reference manual for more details).

Table 21. Main option bytes in STM32L5 and STM32U575/585

Option bit/byte	STM32L5	STM32U575/585
Global TrustZone activation	TZEN: global TrustZone security enable • 0: global TrustZone security disabled • 1: global TrustZone security enabled	
Readout protection (RDP)	RDP level: • 0xAA: L0 (RDP not active) • 0x55: L0.5 (RDP not active, only non-secure debug access possible), only available when TrustZone is active (TZEN = 1) • 0xCC: L2 (device RDP active) • Others: L1 (memories RDP active)	
Reset	• BOR_LEV[2:0]: BOR reset level. These bits contain the V_{DD} supply level threshold that activates/releases the reset. • RST_STOP: reset generation in Stop mode • nRST_STDBY: reset generation in Standby mode • nRST_SHDW: reset generation in Shutdown mode	
	N/A	SRAM134_RST: SRAM1, SRAM3 and SRAM4 erase upon system reset
	SRAM2_RST: SRAM2 erase when system reset	
Watchdog	• IWDG_SW: hardware or software independent watchdog selection • IWDG_STOP: independent watchdog counter freeze in Stop mode • IWDG_STDBY: independent watchdog counter freeze in Standby mode • WWDG_SW: window watchdog selection	
Secure and non-secure boot	• nSWBOOT0: software BOOT0 • nBOOT0 option bit • NSBOOTADD0[24:0]: non-secure boot base-address 0 • NSBOOTADD1[24:0]: non-secure boot base-address 1 • SECBOOTADD0[24:0]: secure boot base-address 0 • BOOT_LOCK: When this bit is set, the boot is always forced to value defined in SECBOOTADD0[24:0].	

Option bit/byte	STM32L5	STM32U575/585
Flash memory secure watermark	Bank 1: • SECWM1_PSTRT[6:0]: first page of the secure area in bank 1 • SECWM1_PEND[6:0]: last page of the secure area in bank 1 • HDP1_PEND[6:0]: last page of HDP area in bank 1 • HDP1EN: Hide protection first area enable Bank 2: • SECWM2_PSTRT[6:0]: first page of the secure area in bank 2 • SECWM2_PEND[6:0]: last page of the secure area in bank 2 • HDP2_PEND[6:0]: last page of HDP area in bank 2 • HDP2EN: Hide protection second area enable	
	Bank 1: • PCROP1_PSTRT[6:0]: first page of PCROP area in bank 1 • PCROP1EN: PCROP1 area enable Bank 2: • PCROP2_PSTRT[6:0]: first page of PCROP area in bank 2 • PCROP2EN: PCROP2 area enable	N/A
Flash memory write protection (WRP) areas	Bank 1: • WRP1A_PSTRT[6:0]: first page of the WPR area A in bank 1 • WRP1A_PEND[6:0]: the last page of the WPR area A in bank 1 • WRP1B_PSTRT[6:0]: first page of the WPR area B in bank 1 • WRP1B_PEND[6:0]: last page of the WPR area B in bank 1 Bank 2: • WRP2A_PSTRT[6:0]: first page of the WPR area A in bank 2 • WRP2A_PEND[6:0]: last page of the WPR area A in bank 2 • WRP2B_PSTRT[6:0]: first page of the WPR area B in bank 2 • WRP2B_PEND[6:0]: last page of the WPR area B in bank 2	
	N/A	UNLOCK, 4 option bits to unlock the following areas: • bank 1 WPR first area A • bank 1 WPR second area B • bank 2 WPR first area A • bank 2 WPR second area B
Flash memory locking keys for RDP level regression	N/A	• OEM1KEY[31:0]: OEM1 least significant bytes key • OEM1KEY[63:32]: OEM1 most significant bytes key • OEM2KEY[31:0]: OEM2 least significant bytes key • OEM2KEY[63:32]: OEM2 most significant bytes key
RAM and ECC enable	N/A	ECC detection and correction enable for the following memories: • BKPRAM_ECC for backup RAM • SRAM2_ECC for SRAM2 • SRAM3_ECC for SRAM3
	SRAM2_PE: SRAM2 parity check enable option bit	Removed, replaced by above ECC options bits
Flash memory banking	SWAP_BANK: used to swap banks	
	DBANK: selection of single or dual-bank Flash with contiguous addresses	DBANK removed

Option bit/byte	STM32L5	STM32U575/585
Flash memory banking	DB256K: dual-bank on 256-Kbyte Flash memories	DUALBANK: dual-bank on 1-Mbyte and 512-Kbyte Flash memories: • 0: single bank Flash with contiguous address in bank 1 • 1: dual-bank Flash with contiguous addresses
I/O speed and pull-up selection	PA15_PUPEN: PA15 pull-up enable: • 0: USB power delivery dead-battery enabled/TDI pull-up deactivated • 1: USB power delivery dead-battery disabled/TDI pull-up activated	
	N/A	• IO_VDD_HSLV: high-speed I/O configuration bit at low V_{DD}. This bit can be set only with V_{DD} is below 2.5 V. • IO_VDDIO2_HSLV: high-speed I/O configuration bit at low V_{DDIO2} voltage. This bit can be set only with V_{DD} is below 2.5 V.

6.3 SRAMs

In STM32L5, the control of SRAM1 and SRAM2 is integrated within the SYSCFG. However, In STM32U575/585, a new peripheral, RAMCFG controller, is dedicated to the control of SRAM1, SRAM2, SRAM3, SRAM4 and BKPSRAM (refer to section 'RAMs configuration controller' in the product reference manual for more details).

The table below compares the embedded SRAMs features in STM32L5 and STM32U575/585.

Table 22. SRAMs in STM32L5 and STM32U575/585

Feature		STM32L5	STM32U575/585
Size (Kbytes)		256 for STM32L552xx/562xx devices: • SRAM1 = 192 • SRAM2 = 64	Up to 786: • SRAM1 = 192 • SRAM2 = 64 • SRAM3 = 512 • SRAM4 = 16 • BKPSRAM = 2
Access by DMA and CPU		Bytes, half-words (16 bits) or full words (32 bits) possible access	
CPU access bus	System bus	SRAM1, SRAM2	SRAM1, SRAM2, SRAM3, SRAM4 and BKPSRAM
	C-bus access	SRAM1, SRAM2	SRAM1, SRAM2, SRAM3
Retention		Either 64 Kbytes or upper 4 Kbytes of SRAM2 can be retained in Standby mode.	Either 8 Kbytes, 56 Kbytes or 64 Kbytes of SRAM2 can be retained in Standby mode
		N/A	BKPSRAM • retention in Standby mode • optional retention in VBAT mode
Security		When the TrustZone security is enabled, all SRAMs are secure after reset.	
		The SRAMs can be programmed as non-secure using the MPCBB with a block granularity of 256 bytes.	The SRAMs can be programmed as non-secure using the MPCBB with a block granularity of 512 bytes.
Hardware erase conditions		All SRAMs are erased in case of RDP level regression from L1 to L0.	All SRAMs are erased by hardware in case of RDP level regression to L0.5 or L0.

Feature	STM32L5	STM32U575/585
Hardware erase conditions	SRAM2 is protected by the tamper detection circuit and is erased by hardware in case of tamper detection.	SRAM2 and optionally BKPSRAM are protected by the tamper detection circuit and are erased by hardware in case of tamper detection.
	SRAM2 is erased by a Backup domain reset.	SRAM2 and BKPSRAM are erased by hardware in case of a Backup domain reset.
Software erase conditions	The SRAM2 erase can be requested by software by setting a single bit in the SYSCFG SRAM2 control and status (SYSCFG_SCSR) register.	All SRAMs erase can be requested by executing a specific software sequence, detailed in section 'RAMCFG' of the product reference manual.
System reset erase	SRAM2 is erased when a system reset occurs if the SRAM2_RST option bit is selected in the Flash memory user option bytes.	
	N/A	SRAM1, SRAM3 and SRAM4 are erased when a system reset occurs if the SRAM134_RST option bit is selected in the Flash memory user option bytes.
WRP	SRAM2 is made of 64 1-Kbyte pages. SRAM2 can be write protected with a page granularity of 1 Kbyte.	
	The write protection can be enabled in SYSCFG SRAM2 write protection register (SYSCFG_SWPR).	Each 1-Kbyte page can be write-protected by setting its corresponding PxWP (x = 0 to 63) bit in RAMCFG registers
Errors detection and correction	Parity check: 4 bits added per 32 bits (1 bit per byte)	ECC: 7 bits added per 32 bits
	N/A	ECC enabled by user option bytes (see Section 6.2 Flash memory)
	One error detection and no error correction	Double-error detection on memory read access Single-error correction
	Parity check supported by the SRAM2 only	ECC supported by SRAM2, SRAM3 and BKPSRAM
	If one parity bit fails, an NMI is generated. Event can be linked to the BRK_IN break input of TIM1, TIM8, TIM15, TIM16 or TIM17.	Interrupts are generated when single and/or double ECC errors are detected: • 2 ECC RAMCFG interrupts • 1 ECC NMI interrupt Interrupts allow the device to exit Sleep, Stop 0 or Stop 1 mode, but not Standby mode.
Read access latency	N/A	3-bit programmable wait-states depending on AHB clock frequency (HCLK) and voltage scaling range (for all SRAMs).

More details about the main features of STM32U575/585 SRAMs are given in the table below.

Table 23. SRAMs main features in STM32U575/585

Feature	STM32U575/585					STM32L5 equivalence
	SRAM1	SRAM2	SRAM3	SRAM4	BKPSRAM	
Size (Kbytes)	192	64	512	16	2	-
LPBAM in Stop 0/1[1]	X	X	X	X	X	N/A
LPBAM in Stop 2	-	-	-	X	-	
Optional retention in Standby mode	-	X	-	-	X	SRAM2 (64 Kbytes)
Optional retention in VBAT mode	-	-	-	-	X	N/A
Erase with RDP regression	X	X	X	X	X	SRAM2
Erase with tamper detection	-	X	-	-	X	SRAM2
Optional erase with system reset	X	X	X	X	-	SRAM2
Software erase	X	X	X	X	X	SRAM2
ECC	-	X	X	-	X	Parity check on SRAM2
Write protection	-	X	-	-	-	Same
Wait states	X	X	X	X	X	N/A

1. *LPBAM: low-power batch acquisition mode.*

6.4 Caches

The STM32U575/585 embed an ICACHE (8 Kbytes) and a DCACHE1 (4 Kbytes) that allows the more efficiently use of the external memory through OCTOSPI and FSMC ports.

The STM32L5 embed only an ICACHE (8 Kbytes) with the same features as the STM32U575/585.

6.5 DMA

STM32L5 and STM32U575/585 have different DMA architectures and features, no compatible registers.

STM32U575/585 DMA modules are called GPDMA (general-purpose DMA) and LPDMA (low-power DMA).The STM32U575/585 embed also a Chrom-ART Accelerator (DMA2D), that is a specialized DMA dedicated to image manipulation (not present in STM32L5).

The table below gives the main differences between GPDMA, LPDMA and DMA modules.

Table 24. DMA features in STM32L5 and STM32U575/585

Features	STM32L5		STM32U575/585	
	DMA1	DMA2	GPDMA1	LPDMA1
Architecture	Each instance of DMA controller is a bus master and system peripheral.			
Number of masters	1 single bidirectional AHB master per instance		Dual bidirectional AHB master	Single bidirectional AHB master

Features	STM32L5		STM32U575/585	
	DMA1	DMA2	GPDMA1	LPDMA1
Linked-List	N/A		• Separately programmed source and destination transfers • Programmable data handling between source and destination • Block-level (programmable number of data bytes) • Linear source and destination addressing: programmable signed address offsets between successive burst transfers	
Linked-List 2D addressing	N/A		• 2D source and destination addressing • Scatter-gather (multi-buffer transfers), data interleaving and de-interleaving via 2D addressing	N/A
Data transfers from source to destination	Peripheral-to-memory, memory-to-peripheral, memory-to-memory and peripheral-to-peripheral			
Number of channels	8	8	16	4
Number of requests/ triggers	127 requests and 23 triggers		114 requests and 44 triggers	16 requests and 32 triggers
	Each DMA controller is connected to DMA requests from AHB/APB peripherals through the DMAMUX.		Same function integrated within GPDMA and LPDMA	
Autonomous data transfer in Sleep and Stop modes	Autonomous data transfers and wakeup during Sleep mode		Autonomous data transfers and wakeup during the low-power modes below	
			Sleep, Stop 0 and Stop 1	Sleep, Stop 0, Stop 1 and Stop 2
TrustZone privileged/ unprivileged	Same features			

6.6 RCC (reset and clock control)

The STM32U575/585 RCC manages clocks and resets of system and peripherals, the same features than the STM32L5, plus some new ones. Registers are not compatible.

The RCC clocks are listed below:

- five internal RC oscillators: HSI16, LSI, MSI (MSIS+MSIK) and HSI48
- two external oscillators (crystal or resonator): HSE and LSE
- three PLLs: PLL1, PLL2 and PLL3

The table below gives an overview of STM32U575/585 and STM32L5 clock sources and resets.

Table 25. RCC features in STM32L5 and STM32U575/585

Feature	STM32L5	STM32U575/585
Safe and flexible reset management without external components	System reset, power reset and Backup domain reset Registers are not compatible.	
Clocks compatibility	STM32L5 clock	Advanced RCC features

Feature	STM32L5	STM32U575/585
Internal clock sources High flexibility on clock source selection to meet consumption and accuracy requirements	4 internal RC oscillators: • HSI16 • MSI • LSI 32 kHz • HSI48	5 internal RC oscillators: • HSI16 (high-speed 16 MHz) • MSIS (multi-speed for system clock) • MSIK (peripheral kernel clock) • LSI 32 kHz (IWDG, optionally drives RTC) • HSI48: 48 MHz for RNG, USB OTG FS and SDMMC
External clock sources High flexibility on clock source selection to meet consumption and accuracy requirements	HSE: high-speed external crystal or user clock with clock security system (CSS) From 4 to 48 MHz	HSE: high-speed external crystal or user clock with clock security system (CSS) From 4 to 50 MHz
	LSE low-speed 32.768 kHz external crystal optionally drives the RTC with clock security system (CSS)	
PLLs	Each of the 3 PLLs provides up to 3 independent outputs. The PLL input can be one of HSI16, HSE and MSI(S).	
	PLL (main PLL)	PLL1
	PLLSAI1	PLL2
	PLLSAI2	PLL3

The table below lists the RCC input/output signals and their mapping on STM32L5 and STM32U575/585. The external kernel clock input for SAI2 digital audio interface (SAI2_EXTCLK) is not present in STM32U575/585.

Table 26. RCC pin names in STM32L5 and STM32U575/585

Alternate function	STM32L5 pin name	STM32U575/585 pin name
NRST	NRST	
OSC32_IN	PC14	
OSC32_OUT	PC15	
OSC_IN	PH0	
OSC_OUT	PH1	
MCO	PA8	
LSCO	PA2	
SAI1_EXTCLK	PA0/PB0	
SAI2_EXTCLK	PA2/PC9	N/A

The table below details the RCC clock sources for STM32U575/585 compared to STM32L5.

Table 27. Clock sources in STM32L5 and STM32U575/585

Clock source	STM32L5	STM32U575/585
System clock	• MSI, HSI16, HSE or PLL • 110 MHz maximum frequency • 4 MHz after reset using MSI	• MSIS, HSI16, HSE or PLL • 160 MHz maximum frequency • 4 MHz after reset using MSI
HSE	4 to 48 MHz	4 to 50 MHz
LSE	32.768 kHz, configurable drive/consumption, available in Backup domain (VBAT)	

Clock source	STM32L5	STM32U575/585
LSI	32 kHz RC, low consumption, high accuracy (refer to electrical characteristics section of the datasheet)	
MSI	MSI 1 output clock (MSI) with 12 frequency ranges	MSI = MSIS (system) + MSIK (kernel) 2 output clocks (MSI + MSIK) with 16 frequency ranges
	• Multi-speed RC factory and user trimmed • 4 MHz default clock value after reset or Shutdown mode • low-power oscillator with programmable frequency up to 48 MHz MSI can be selected as system clock after wakeup from Stop modes.	
MSI + PLL + LSE high accuracy	When used in PLL-mode with LSE: • MSI provides a very accurate clock source that can be used by the USB_FS. • MSI feeds the PLL to run the system at 80 MHz maximum speed .	When used in PLL-mode with LSE: • The MSI provides a very accurate clock source that can be used by the USB FS. • The MSI feeds the PLL to run the system at **160** MHz maximum speed.
MSI calibration	Hardware auto-calibration from LSE and software calibration possible	
HSI16	• generated from an internal 16 MHz RC oscillator • 16 MHz RC factory and user trimmed • can be used as a backup clock source (auxiliary clock) if HSE crystal oscillator fails • can be selected as system clock after wakeup from Stop modes	
HSI48	48 MHz RC independent oscillator	
	Can drive RNG, SDMMC and USB FS	Can drive RNG, SDMMC and USB **OTG** FS
Clock-out capabilities MCO and LSCO	One of the following clock signals can be selected as MCO: LSI, LSE, SYSCLK, HSI16, HSI48, HSE, PLLCLK or MSI.	One of the following clock signals can be selected as MCO: LSI, LSE, SYSCLK, HSI16, HSI48, HSE, PLLCLK, **MSIS or MSIK**.
	One of the following clock signals can be selected as LSCO: LSI or LSE. This output remains available in Stop 0, Stop 1, Stop 2 and Standby modes.	
Clock measurement and calibration using TIM15, TIM16 or TIM17	All on board clock sources. The frequency can be measured by mean of the TIM15, TIM16 or TIM17 channel 1 input capture. • Calibration using LSE: HSI16 and MSI calibration using **LSE** and TIM15/TIM16/TIM17 • Calibration using HSE: – HSI16 and MSI calibration using HSE and TIM16/TIM17 – LSI calibration using **HSE** and TIM16/TIM17	
Clock measurement and calibration using LPTIM1 and LPTIM2	N/A	All on board clock sources. The frequency can be measured by mean of the LPTIM1 or LPTIM2 channel 2 input capture. • Calibration using LSE: HSI16 and MSI calibration using **LSE** and LPTIM2 • Calibration using HSE: – HSI16 and MSI calibration using HSE and LPTIM2 – LSI calibration using HSE and LPTIM1
Interrupts	Equivalent interrupt vector to the one below is available for secure events. The RCC secure interrupt vector is used only when TrustZone is enabled.	
	CSS (linked to NMI IRQ)	
	LSECSS	HSECSS
	MSIRDY	MSISRDY and MSIKRDY

Clock source	STM32L5	STM32U575/585
Interrupts	PLLRDY, PLLSAI1RDY and PLLSAI2RDY	PLL1RDY, PLL2RDY and PLL3RDY
	N/A	SHSIRDY and HSI48RDY
	LSIRDY, LSERDY, HSIRDY and HSERDY	

6.6.1 PLL

The PLL architecture of the STM32U575/585 supports the same than STM32L5 but with the updated features detailed in the table below.

Table 28. PLL features in STM32L5 and STM32U575/585

Feature	STM32L5	STM32U575/585
Number of PLL	RCC features three completely independent PLLs: • PLL (main PLL) • PLLSAI1 (for SAI1 device) • PLLSAI2 ((for SAI2 device)	RCC features three completely independent PLLs: • PLL (main PLL) used to provide clocks to the CPU and to some peripherals • PLL2 and PLL3 used to generate the kernel clock for dedicated peripherals
Input/output frequencies	• Input frequency range: 4 to 16 MHz • Each PLL offers three outputs with post-dividers. • The internal PLLs can be used to multiply the HSI16, HSE or MSI output clock frequency.	
	• The output frequency must not exceed 110 MHz.	• The output frequency must not exceed 160 MHz.
sigma-delta (ΣΔ) modulator	N/A	13-bit sigma-delta (ΣΔ) modulator, used to fine-tune the VCO frequency by steps of 11 to 0.3 ppm The ΣΔ modulator can be updated on-the-fly, without generating frequency overshoots on PLLs outputs.
Integer/fractional mode	Capability to work in integer mode only: each PLL selected source is divided by a factor from 1 to 8.	Capability to work either in integer or in fractional mode

6.6.2 Bus frequencies versus voltage scaling

The table below lists the maximum frequencies of internal bus in STM32U575/585 and STM32L5, depending on the product voltage range.

Table 29. Bus max frequency versus voltage scaling in STM32L5 and STM32U575/585

Product voltage range	STM32L5 AHB, AHB1, APB1, APB2 max frequency (MHz)	STM32U575/585 AHB1, AHB2, APB1, APB2, AP3 max frequency (MHz)
Range1	110	160
Range2	80	110
Range3	26	55
Range4	N/A	25

6.6.3 CSS (clock security system)

The table below lists the CSS updates of the STM32U575/585 compared with STM32L5.

Table 30. CSS in STM32L5 and STM32U575/585

CSS clock source	STM32L5	STM32U575/585
CSS on HSE	Same features	
CSS on LSE modes	Works in all modes **except** VBAT.	Works in all modes **including VBAT**
CSS on LSE detection mode	Clock missing detection	Under-frequency and over-frequency detection
	The CSS on LSE detection event is connected to the internal tamper of the TAMP peripheral. A tamper event and the associated interrupt wake up the system from low-power modes. The software can handle the detection tasks.	

6.6.4 Specific ADC and DAC clocks features

The STM32U575/585 RCC clocks driving ADC and DAC have the same features than the STM32L5, in particular:

- If ADC or DAC is precisely triggered by a TIMx timer without any uncertainty, the HCLK must be selected as ADC and DAC kernel clock source. The other clock sources are asynchronous to TIMx timers. The LPTIMx timers are also asynchronous.
- The DAC requires an additional low-power clock (LSI or LSE) to operate in sample-and-hold mode, available in Stop mode. This clock is selected with DAC1SEL in RCC_CCIPR3.

6.6.5 RTC and TAMP clock

The table below lists the features of RTC and TAMP clock sources for STM32L5 and STM32U575/585.

Table 31. RTC and TAMP clock in STM32L5 and STM32U575/585

Feature	STM32L5	STM32U575/585
Clock source for RTC and TAMP	HSE / 32, LSE or LSI	
Only the backup registers used in TAMP with tampers in edge detection mode	No kernel clock required	
Backup domain active clocks	LSE	LSE and LSI

6.6.6 Timer and watchdog clock sources

STM32L5 and STM32U575/585 share the same features for timer and watchdog clock sources.

The timer clock frequencies are automatically defined by hardware, with the following cases:

- If the APB prescaler equals one, the timer clock frequencies are set to the APB domain frequency.
- Otherwise, they are set to twice (x 2) the APB domain frequency.

If the independent watchdog (IWDG) is started by either hardware option or software access, the LSI oscillator is forced on and cannot be disabled. After the LSI oscillator temporization, the LSI 32 kHz clock is provided to the IWDG.

6.6.7 Peripherals clock gating and reset

Since the address mapping of some peripherals has been changed in the STM32U575/585 compared to the STM32L5, different registers must be used to [enable/disable] or [enter/exit] the peripheral [clock] or [from Reset mode]. The STM32U575/585 have in addition the [enable/disable] of the autonomous mode in SmartRun domain.

The table below shows the RCC registers used for peripheral access configuration for STM32U575/585 and STM32L5.

Table 32. RCC clock and reset registers for STM32L5 and STM32U575/585

Register	STM32L5	STM32U575/585
AHB: [enter/exit] AHB peripherals from Reset	• RCC_ AHB1RSTR • RCC_ AHB2RSTR • RCC_ AHB3RSTR	• RCC_ AHB1RSTR • RCC_ AHB2RSTR • RCC_ AHB3RSTR • RCC_ AHB4RSTR
APB: [enter/exit] APB peripherals from Reset	• RCC_ APB1RSTR1 • RCC_ APB1RSTR2 • RCC_ APB2RSTR	• RCC_ APB1RSTR1 • RCC_ APB1RSTR2 • RCC_ APB2RSTR • RCC_ APB3RSTR
AHB: [enable/disable] the AHB peripheral clock	• RCC_ AHB1ENR • RCC_ AHB2ENR • RCC_ AHB3ENR	• RCC_ AHB1ENR • RCC_ AHB2ENR • RCC_ AHB3ENR • RCC_ AHB4ENR
APB: [enable/disable] the APB peripheral clock	• RCC_ APB1ENR1 • RCC_APB1ENR2 • RCC_ APB2ENR	• RCC_ APB1ENR1 • RCC_ APB1ENR2 • RCC_ APB2ENR • RCC_ APB3ENR
AHB: [enable/disable] the AHB peripheral clock in Sleep mode	• RCC_AHB1SMENR • RCC_AHB2SMENR • RCC_AHB3SMENR	• RCC_ AHB1SMENR • RCC_ AHB2SMENR • RCC_ AHB3SMENR • RCC_ AHB4SMENR
APB: [enable/disable] the APB peripheral clock in Sleep mode	• RCC_APB1SMENR1 • RCC_APB1SMENR2 • RCC_APB2SMENR	• RCC_ APB1SMENR1 • RCC_ APB1SMENR2 • RCC_ APB2SMENR • RCC_ APB3SMENR
SRD(SmartRun domain): [enable/disable] the peripheral in autonomous mode enable in Stop 0, Stop 1 and Stop 2 modes	N/A	• RCC_ SRDAMR

Caution: After the enable bit is set, the clock is active after two cycles of the peripheral bus clock.

The SMEN bit of the peripheral must be set to allow the generation of an interrupt capable to wake up the device from Stop mode. This is not necessary when the peripheral wakeup interrupt is generated though the EXTI.

6.6.8 Peripheral clock source migration

This section provides the differences between the peripheral clock sources in STM32U575/585 and STM32L5 Series.

Table 33. Peripheral clock sources in STM32L5 and STM32U575/585

Peripheral	STM32L5	STM32U575/585
IWDG	LSI RC 32 kHz	LSI RC 32 kHz or 250 Hz
WWDG	PCLK1	
UCPD1	HSI16 RC	
RTC	LSE, LSI, HSE/32	

Peripheral	STM32L5	STM32U575/585
LPTIM1, 3, 4	HSI16, LSE, LSI, PCLK1 (APB1 clock), external clock mapped on LPTIMx_IN1	HSI16, LSE, LSI, MSIK
LPTIM2		HSI16, LSE, LSI,
TIMx (x = 2..7)	PCLK1	
TIMx (x = 1,8,15,16,17)	PCLK2	
USARTx (x = 2..5)	LSE, HSI16, PCLK1, SYSCLK	
USART1	LSE, HSI16, PCLK2, SYSCLK	
LPUART1	HSI16, LSE, PCLK1, SYSCLK	HSI16, LSE, MSIK, SYSCLK
SPI1	PCLK2	HSI16, MSIK, PCLK2, SYSCLK
SPI2	PCLK1	HSI16, MSIK, PCLK1, SYSCLK
SPI3	PCLK1	HSI16, MSIK, PCLK3, SYSCLK
I2Cx (x = 1, 2, 4)	HSI16, PCLK1, SYSCLK	HSI16, MSIK, PCLK1, SYSCLK
I2C3		HSI16, MSIK, PCLK3, SYSCLK
OCTOSPI1	MSI, PLL48M1CLK, SYSCLK	MSIK, pll1_q_ck, pll2_q_ck, SYSCLK
OCTOSPI2	N/A	
SAES		SHSI RC, SHSI RC/2
ADF1, MDF1	HSI16, MSI, PLLSAI1CLK, PLLSAI2CLK, PLLSAI3CLK, SAI1_EXTCLK(1)	AUDIOCLK (external), MSIK, pll1_p_ck, pll3_q_ck
SAI2	HSI16, MSI, PLLSAI1CLK, PLLSAI2CLK, PLLSAI3CLK, SAI1_EXTCLK	AUDIOCLK (external), HSI16, pll1_p_ck, pll2_p_ck, pll3_p_ck
SDMMC1	HSI48, MSI, PLL48M1CLK (main PLL VCO), PLL48M2CLK (PLLSAI1 VCO), PLLSAI3CLK	HSI48, MSIK, pll1_p_ck, pll1_q_ck, pll2_q_ck
SDMMC2	N/A	
OTG_FS	HSI48, MSI, PLL48M1CLK, PLL48M2CLK(2)	HSI48, MSIK, pll1_q_ck, pll2_q_ck
RNG	HSI48, MSI, PLL48M1CLK, PLL48M2CLK	HSI16, HSI48, HSI48/2
ADC1, ADC4	PLLADC1CLK, SYSCLK	HCLK, HSE, HSI16, MSIK, pll2_r_ck, SYSCLK
DAC	PCLK1	
DAC1 Sample and Hold		LSE, LSI
FDCAN1,2	HSE, PLL48M1CLK, PLLSAI1CLK	HSE, PCLK1, pll1_q_ck, pll2_p_ck
LPGPIO1	N/A	HCLK
GPIOx	HCLK	
VREFBUFF	PCLK2	PCLK3
COMP	PCLK2	
OPAMP	PCLK1	
FSMC	HCLK	
DLYB	N/A	HCLK
OTFDEC1	HCLK	
OTFDEC2	N/A	HCLK
OCTOSPIM		
PKA	HCLK	

Peripheral	STM32L5	STM32U575/585
AES	HCLK	
PSSI	N/A	HCLK
DCMI		
TSC	HCLK	
CRC		
FMAC	N/A	HCLK
CORDIC		
CRS	HSI48	

1. *In DFSDM.*
2. *USB_FS*

6.6.9 System clock after wakeup

This section provides the differences between the system clock used after wakeup in STM32L5 and STM32U575/585 devices.

Table 34. System source after wakeup in STM32L5 and STM32U575/585

Power mode	STM32L5	STM32U575/585
Sleep (Sleep-now or Sleep-on-exit)	Same clock as before entering Sleep mode	
Stop 0, Stop 1, Stop 2	HSI16 or MSI (same frequency as before entering Stop mode)	HSI16 or MSIS (same frequency as before entering Stop mode, limited to 24 MHz)
Stop 3	N/A	
Standby (with SRAM2_4 Kbytes, with SRAM2_full, or without retention)	MSI (from 1 to 8 MHz)	MSIS (from 1 to 4 MHz)
Shutdown	MSI (4 MHz)	MSIS (4 MHz)

6.6.10 Autonomous mode in STM32U575/585

In STM32U575/585,some peripherals support an autonomous mode in Stop 0, Stop 1 and Stop 2 modes:

- Peripherals are able to generate a **kernel clock** request and a **AHB/APB bus clock** request when needed, even in Stop mode.
- The MSI or HSI16 oscillator is woken up.
- In autonomous mode with DMA, the AHB/APB clocks as well as the oscillator (HSI16 or MSI) are automatically switched off as soon as the transfer is finished. The device automatically goes back in Stop mode.
- If the autonomous peripheral is configured with interrupt enabled, the interrupt wakes up the device into Run mode.

The autonomous mode is not supported by STM32L5 peripherals. On the opposite, they have the following limited capabilities in Stop mode when needed:

- If HSI16 is selected as clock source for U(S)ARTs, LPUARTs and I2C, HSI16 can be enabled by these peripherals in Stop 0, Stop 1 or Stop 2 mode.
- The LSE can remain always ON in Stop mode, with no on-the-fly activation capability, when it drives U(S)ARTs and LPUARTs.

The table below lists the main features of the autonomous mode supported by the STM32U575/585 only.

Table 35. STM32U575/585 autonomous mode

Feature	Description
CPU domain (CD)	• Autonomous peripherals in Stop 0 and Stop 1 modes only • Enabled if both xxEN and xxSMEN bits of the peripheral are set (xx = instance name) • Autonomous peripherals mapped on AHB1, AHB2, APB1 and APB2 • GPDMA1 is associated. • SRAM1, SRAM2, SRAM3 are associated. • SRAM4 belongs to SmartRun domain (SRD) but can be addressed by GPDMA 1 in Stop 0 and Stop 1 modes.
SmartRun domain (SRD)	• Autonomous peripherals in Stop 0, Stop 1 and Stop2 modes • Enabled if both xxEN and xxSMEN bits, plus the xxAMEN bit of the peripheral in the RCC SRD peripheral autonomous mode register (RCC_SRDAMR). • Autonomous peripherals mapped on AHB3 or APB3 • LPDMA1 is associated. • SRAM4 is associated.
Autonomous peripherals in CD	• U(S)ARTx (x = 1 to 5) • SPIx (x = 1, 2) • I2Cx (x = 1, 2) • LPTIM2 • MDF1 • GPDMA1
Autonomous peripherals in SRD	• LPUART1 • SPI3 • I2C3 • LPTIMx (x = 1, 3, 4) • ADF1 • DAC1 • ADC4 • LPDMA1
Autonomous peripheral requesting its kernel clock in Stop 0, Stop 1 or Stop 2 mode	• The internal oscillator (HSI16 or MSI) is woken up, if it was off. • The kernel clock is propagated only to the peripheral requesting it. • When the peripheral releases its kernel clock request, the HSI16 or MSI is switched off if no other peripheral requests it.
Autonomous peripheral in CD, requesting its bus clock in Stop 0 or Stop 1 mode	• The internal oscillator (HSI16 or MSI) is woken up, if it was off. • The system clock is propagated to all peripherals configured with both xxEN and xxSMEN bits set.
Autonomous peripheral belonging to SRD, requesting its bus clock in Stop 2 mode	• The internal oscillator (HSI16 or MSI) is woken up if it was off. • The HCLK3 and PCLK3 clocks are propagated to all peripherals of the SmartRun domain configured with xxEN, xxSMEN and xxAMEN set.
Forcing MSIK or HSI16 ON in Stop 0, Stop1 or Stop 2 mode	• Can be done by configuring MSIKERON or HSIKERON is RCC_CR. • The oscillator is propagated only to the kernel clock of the enabled autonomous peripherals with this oscillator selected as kernel clock. • This allows the peripheral baud rates or conversion rates increase, as there is no need to wait for the oscillator wakeup time when the peripheral requests its kernel clock.
LSE or LSI as kernel clock	• The LSE or LSI selected as peripheral kernel clock remains always ON in Stop mode.
Forcing AHB3 and APB3 clocks ON in SRD domain	• Performed by setting the SRDRUN bit in PWR_CR2 • Allows the LPDMA1 latency to be improved as no oscillator wakeup time when the peripheral requests its bus clock.

6.6.11 Low-power modes

The table below lists the main low-power modes and main clock sources of STM32L5 and STM32U575/585.

Table 36. Low-power modes in STM32L5 and STM32U575/585

Feature		STM32L5	STM32U5
Software enable/disable		AHB and APB peripheral clocks, including DMA clock, can be disabled by software.	
Sleep mode		• Sleep mode stops the CPU clock. • The memory interface clocks can be stopped by software during Sleep mode. • AHB to APB bridge clocks are disabled by hardware during Sleep mode, when all the clocks of the peripherals connected to them are disabled.	
Stop modes		Stop 0, Stop 1, Stop 2	Stop 0, Stop 1, Stop 2, Stop 3
		Stop all the clocks in the V_{CORE} domain and disable the PLLs, HSI16, HSI48, MSI and HSE oscillators.	
Stop modes and Autonomous	Autonomous mode	N/A	Autonomous mode in Stop 0, Stop 1 and Stop 2 modes
	HSI or MSI clock source	All U(S)ARTs, LPUARTs and I2Cs can enable the HSI16 even when the MCU is in Stop mode.	HSI16 or MSI can be switched ON if the peripheral requests it for autonomous mode purpose, or to generate a wakeup interrupt.
	LSE clock source	All U(S)ARTs and LPUARTs can be driven by the LSE oscillator when the system is in Stop mode.	
		The LSE remains always ON in Stop mode.	LSI and LSE remain active in Stop mode.
Standby and Shutdown modes		These modes stop all the clocks in the V_{CORE} domain and disable the PLLs, HSI16, HSI48 (U5 only), MSI and HSE oscillators.	
CPU Deepsleep mode		This mode can be overridden for debugging.	
Exiting Stop modes		• When exiting Stop modes, the system clock is either MSIS (MSI for STM32L5) or HSI16, depending on the software configuration. • The user trim of HSI16 is kept.	
		N/A	Internal oscillators (other than HSI16 or MSI) can be automatically woken up in addition to the one used by the system clock, in order to avoid waiting for the other oscillator wakeup time when the device is back in Run mode
Leaving Standby and Shutdown modes		The system clock is MSI when leaving these modes.	The system clock is MSI(S) when leaving these modes.
		The MSI frequency at wakeup from Standby mode is configured from 1 to 8 MHz.	The MSIS and MSIK frequency at wakeup from Standby mode is configured from 1 to 4 MHz.
		The MSI frequency at wakeup from Shutdown mode is 4 MHz. The user trim is lost.	
Low-power modes and Flash memory programming		• If a Flash memory programming operation is ongoing, Stop, Standby or Shutdown mode entry is delayed until the Flash memory interface access is finished. • If an access to the APB domain is ongoing, Stop, Standby or Shutdown mode entry is delayed until the APB access is finished.	
		N/A	If an autonomous peripheral generates a system clock request, Stop, Standby or Shutdown mode entry is delayed until the system clock request is released.

6.6.12 RCC security and privilege functional description

When the TrustZone security is activated, the RCC is able to secure RCC configuration and status bits from being modified by non-secure accesses. The RCC_SECCFGR register is used in both STM32U5 and STM32L575/585 to prevent non-secure access to read or modify the items listed in the table below.

Table 37. Secured RCC items in STM32L5 and STM32U575/585

Feature	STM32L5	STM32U575/585
Clock sources configuration and status bits	HSE, HSE-CSS, HSI, MSI, LSI, LSE, LSE-CSS, HSI48	
PLLs , AHB and APB prescaler configuration and status bits	Main PLL, PLLSAI1, PLLSAI2, AHB	PLL1, PLL2, PLL3, AHB and **APB**
System and independent clocks	SYSCLK and HSI48 source clock selection and status bits	
Clock out capability	MCO and LSCO	
Wake up configuration and status bits	STOPWUCK	STOPWUCK and STOPKERWUCK
Remove reset flog settings	RMVF	

When a peripheral is configured as secure, its related clock, reset, clock source selection, and clock enable during low-power modes control bits are also secure. The registers listed in the table below have a secured access for STM32L5 and STM32U575/585.

Table 38. RCC secure-access registers in STM32L5 and STM32U575/585

STM32L5	STM32U575/585
RCC_AHBxENR, RCC_APBxENR, RCC_AHBxSMEN, RCC_APBxSMEN, RCC_SRDAMEN, RCC_CCIPR, RCC_CCIPR2	
N/A	RCC_CCIPR3 and RCC_BDCR

The security configuration bits in RCC_SECCFGR are similar in STM32LU5 and STM32L575/585. Moreover, when one security configuration bit is set, some configuration and status bits are secured.

The RCC registers may contain secure and non-secure bits (refer to the product reference manual for more details).

6.6.13 RCC privilege protection modes

In STM32U575/585, there is dedicated register for privileged and unprivileged access: RCC_PRIVCFGR (SPRIV and NSPRIV bits). In STM32L5, there only one dedicated bit in RCC_CR register (PRIV).

By default, after a reset, all RCC registers can be read or written with privileged and unprivileged access, except RCC_PRIVCFGR (PRIV bit in STM32L5) that can be written with privileged access only.

RCC_PRIVCFGR can be read by secure and non-secure, privileged and unprivileged access.

The table below summarizes the possible software configuration in STM32L5 and STM32U575/585.

Table 39. Privileged and unprivileged accesses in STM32L5 and STM32U575/585

Feature	STM32L5	STM32U575/585
Software RCC privileged configuration	Bit configuration: PRIV (bit 31 of RCC_CR) After reset, this PRIV bit can be written with privileged access only.	Register configuration RCC_PRIVCFGR: • SPRIV: RCC secure functions privilege configuration • NSPRIV: RCC non-secure functions privilege configuration After reset, RCC_PRIVCFGR can be written with privileged access only.

Feature	STM32L5	STM32U575/585
Dedicated bit for secure privileged access	N/A	• SPRIV can be written with secure privileged access only. • SPRIV configures the privileged access of all RCC secure functions.
Dedicated bit for secure and non-secure privileged access		• NSPRIV can be written with privileged access only, secure or non-secure. • NSPRIV configures the privileged access of all RCC non-secure functions.

6.7 Power (PWR)

STM32U575/585 and STM32L5 share the same PWR features, except:

- the regulator bypass option that is present in STM32L5 only
- the following STM32U575/585 features, not covered by STM32L5:
  - SMPS (DC-DC) power converter function in parallel to LDO, with on-the-fly selection, for optimum power consumption and noise filtering
  - LPBAM (low-power batch acquisition) mode, down to Stop 2 mode, ensuring peripheral DMA transfers in autonomous mode
  - SRAM power down in Stop with 64-Kbyte max granularity
  - Stop 3 mode
  - Up to 24 multiplexed wakeup pins from Stop 3, Standby and Shutdown modes
  - Registers privilege configuration for secure distinct from non-secure

6.7.1 Power-supply pins

The power-supply pin-numbers are not fully aligned in STM32L5 and STM32U575/585. The following tables include only the common packages and differences between pins.

Table 40. Power-supply pins in STM32L5 and STM32U575/585 (packages with SPMS)

Pin name		Pin number			
STM32L5	STM32U75/585	LQFP64_SMPS	LQFP100_SMPS	UFBGA132_SMPS	LQFP144_SMPS
VDDSMPS	VLXSMPS	28	47	M9	68
VLXSMPS	VDDSMPS	29	46	M10	69
VSS	VDD11	31	49	M11 (V15SMPS in L5)	71
VSS	VDD11	62	98	B4 (V15SMPS in L5)	142
V15SMPS	VSS	32	50	M11 (VDD11 in U5)	72
V15SMPS	VSS	63	99	B4 (VDD11 in U5)	143

Table 41. Power-supply pins in STM32L5 and STM32U575/585 (packages without SPMS)

Pin name		Pin number				
STM32L5	STM32U75/585	LQFP48	LQFP64	LQFP100	UFBGA132	LQFP144_SMPS
PB11	VCAP	22	30	47	M9	68

The table below details power-supply pins that are specific to STM32U575/585.

Table 42. STM32U575/585 specific power-supply pins

Pin name	STM32L5	STM32U575/585
WKUPx	WKUPx (x = 1 to 5) input wakeup pins	WKUPx (x = 1 to 8) input wakeup pins Up to 24 multiplexed wakeup pins from Stop 3, Standby and Shutdown modes
CSLEEP	N/A	CSLEEP output MCU in Sleep mode
CDSTOP		CDSTOP output CPU domain in Stop mode
SRDSTOP		SRDSTOP output SmartRun domain in Stop mode (no system clock running)

6.7.2 PWR main features

The table below details PWR main features for STM32L5 and STM32U575/585.

Table 43. PWR in STM32L5 and STM32U575/585

Feature		STM32L5	STM32U575/585
Power supplies and supply domains	V_{DD}	V_{DD} = 1.71 V to 3.6 V	
	Core (V_{CORE})	1.0 V to 1.28 V depending on power ranges	0.9 V to 1.28 V depending on power ranges
	Backup (V_{BAT})	V_{BAT} = 1.55 V to 3.6 V	
	V_{DDA}	V_{DDA} min value: • 1.62 V for ADCs and COMPs • 1.8 V for DACs and OPAMPs • 2.4 V for VREFBUF V_{DDA} max value = 3.6 V	V_{DDA} min value: • 1.62 V for ADCs, COMPs, DACs and OPAMPs • 2.4 V for VREFBUF V_{DDA} max value = 3.6 V
	Internal SMPS	Supply for the SMPS power stage (available only on SMPS packages)	
		V_{DDSMPS} = 2 V to 3.6 V	V_{DDSMPS} = 1.71 V to 3.6 V
	V_{DDIO2} on PG[15:2]	V_{DDIO2} = 1.08 V to 3.6 V	
	V_{DDUSB} for USB transceiver	V_{DDUSB} = 3.0 V to 3.6 V	
	V_{REF-}, V_{REF+}	• V_{REF+} around 2.048 V when V_{DDA} ≥ 2.4 V • V_{REF+} around 2.5 V when V_{DDA} ≥ 2.8 V	
		N/A	• V_{REF+} around 1.8 V when V_{DDA} ≥ 2.1 V • V_{REF+} around 1.5 V when V_{DDA} ≥ 1.8 V
System supply-voltage regulation		SMPS step-down converter or LDO linear voltage regulator SMPS fast startup configuration option available	
		External SMPS (regulator bypass)	N/A
		SMPS, LDO and bypass selected by the user	SMPS and LDO function in parallel, with on-the-fly selection
		SMPS enabled and configured by the user in: • HPM (high-power mode) used in range 0, 1 and 2 • LPM (low-power mode used in range 2	LDO or SMPS can be used in all voltage scaling ranges, and in all Stop modes.

Feature	STM32L5	STM32U575/585
System supply-voltage regulation	• Bypass mode	
	HPM is the default selected mode after POR reset.	After reset, the regulator is the LDO in range 4.
	When exiting low-power mode, the SMPS is set to the mode selected prior to the low-power mode selection.	When exiting Stop or Standby mode, the voltage range is range 4.
Dynamic voltage scaling ranges	Three power ranges: • Range 0: high performance V_{CORE} 1.28 V, sysclk 110 MHz • Range 1: medium performance V_{CORE} 1.2 V, sysclk 80 MHz • Range 2: low-power range V_{CORE} 1.0 V, sysclk 26 MHz	Four power ranges: • Range 1: high performance V_{CORE} 1.2 V, sysclk 160 MHz • Range 2: medium performance V_{CORE} 1.1 V, sysclk 100 MHz • Range 3: medium low-power range V_{CORE} 1.0 V, sysclk 50 MHz • Range 4: low-power range V_{CORE} 0.9 V, sysclk 24 MHz
Power-supply supervision	• POR/PDR • BOR monitor • PVD monitor • PVM monitor (VDDA, VDDUSB, VDDIO2) • Out of functional range temperature monitor	
	N/A	Out of functional range core domain monitor (range 2 and range 3 only)
	Upper V_{DD} voltage threshold monitor	Out of functional range Backup domain voltage monitor
BOR monitoring	• BOR is active in all power modes except Shutdown mode, and cannot be disabled. • Five BOR thresholds can be selected through option bytes. • Set the BOR in ultra-low-power mode to further reduce the current consumption.	
	BOR monitors only V_{DD}.	BOR monitors the Backup domain supply voltage: V_{DD} when present or V_{BAT} otherwise.
Programmable voltage detector (PVD)	• Monitors V_{DD} by comparing it to above/below threshold . • Can generate an interrupt if enabled through EXTI registers. • Can be set in ultra-low-power mode during Stop 2 and Stop 3 modes, to further reduce the current consumption. • Can remain active in Stop 0, Stop 1, Stop 2 modes.	
	PVD interrupt can wake up from the Stop mode.	
Peripheral voltage monitoring (PVM)	• V_{DDA}, V_{DDIO2} and V_{DDUSB} can be independent from V_{DD}. • Each PVM output is connected to an EXTI line and can generate an interrupt if enabled. • Four PVM thresholds are defined for these independent power supplies: – UVM monitors the V_{DDUSB}. – IO2VM monitors the PG[15:2] supply V_{DDIO2}. – AVM1 and AVM2 are two thresholds that monitor the analog supply V_{DDA}.	

6.7.3 Power modes

The ultra-low-power STM32U575/585 devices support eight low-power modes to achieve the best compromise between low-power consumption, short startup time, available peripherals and available wake-up sources. The table below shows the related STM32U575/585 power modes compared to STM32L5 ones.

Table 44. Power modes in STM32L5 and STM32U575/585

Power mode	STM32L5	STM32U575/585
Run mode	• Prescalers can be programmed for slowing down system clocks (SYSCLK, HCLK, PCLK) and peripheral clocks before entering the sleep mode. • Peripheral clock gating: HCLK and PCLK for individual peripherals and memories can be stopped.	
Low-power run mode	• Regulator can be configured in low-power mode. • System clock frequency is reduced below 2 MHz. • Code is executed from SRAM or from Flash memory.	This mode is replaced by range in voltage scaling: system clock frequency up to 24 MHz
Sleep mode	CPU clock off. All peripherals can run and wake up the CPU when an interrupt or an event occurs.	
Low-power sleep mode	This mode is entered from low-power run mode.	This mode is replaced by the range 4 in voltage scaling.
Stop modes	Stop0, Stop1 and Stop2 modes	Stop 0, Stop 1, Stop 2 and Stop 3 modes
	SRAM1 or SRAM2	SRAM1, SRAM2, SRAM3 or SRAM4
	N/A	SRAM blocks can be powered down to reduce consumption.
	• SRAMs and all registers content are retained. • All clocks in the V_{CORE} domain are stopped. • PLL, MSI (MSIS and MSIK) RC, HSI16 RC and HSE crystal oscillators are disabled. • LSE or LSI is still running. • RTC can remain active.	
	Some peripherals can enable the HSI16 RC to detect their wakeup condition.	Some peripherals are autonomous and can operate in Stop mode: • request their kernel clock and their bus (APB or AHB) when needed • transfer data with DMA
	Stop 0 and Stop 1 offer largest number of active peripherals and wakeup sources, smaller wakeup time but a higher consumption than Stop 2.	
	In Stop 2, the V_{CORE} domain is put in a lower leakage mode.	In Stop 2 and Stop 3, the V_{CORE} domain is put in a lower leakage mode.
	N/A	Stop 3 is the lowest power mode with full retention: Functional peripherals and sources of wakeup are reduced to the same ones than in Standby mode.
	The system clock, when exiting Stop mode, can be either MSI up to **48** MHz or HSI16, depending on the software configuration.	The system clock, when exiting Stop mode, can be either MSIS up to **24** MHz or HSI16, depending on software configuration.
Standby mode	• V_{CORE} domain is powered off. • PLL, MSI (MSIS and MSIK in case of U5), HSI16 and HSE are also switched off. • RTC can remain active. • BOR remains always active.	

Power mode	STM32L5	STM32U575/585
Standby mode	Wakeup sources: • WKUPx pin edge, RTC event, external reset in NRST pin, IWDG reset, BOR reset • A tamper detection can be raised either due to external pins or due to an internal failure detection.	
	5 WKUPx pin edge sources	24 WKUPx pin edge sources
	Standby system clock after wakeup: MSI from 1 MHz up to 8 MHz.	Standby system clock after wakeup: MSIS up to 4 MHz.
	Standby and I/Os: • I/Os are by default in floating state. • The state of each I/O can be selected by software: I/O with internal pull-up, internal pull-down or floating.	
	The full SRAM2 or only the upper 4 Kbytes can be retained.	The full SRAM2, 8 Kbytes or 56 Kbytes can be retained.
Shutdown mode	• V_{CORE} domain is powered off. • All clocks in the V_{CORE} domain are stopped. PLL, MSI, HSI16, LSI and HSE are disabled. • LSE can be kept running. • RTC and TAMP can remain active. • BOR is not available (no power monitoring). • Switch to the Backup domain is not possible. • The system clock, when exiting Shutdown mode, is MSI at 4 MHz.	
Auto-wakeup from a low-power mode	RTC can be used to wake up the MCU from a low-power mode without depending on an external interrupt (auto-wakeup mode).	

6.7.4 Low-power batch acquisition mode (LPBAM)

This mode is a key feature of STM32U575/585 in order to reduce power consumption. Without any software running, LPBAM allows peripherals to be functional and autonomous in Stop 0, Stop 1 and Stop 2 modes. Peripherals request their kernel clock and their bus (APB or AHB) when needed in order to transfer data with DMA. The assigned DMA can be LPDMA1 or GPDMA1 as specified in the table below. For more details about this mode, refer to product reference manual.

Table 45. STM32U575/585 peripherals to DMA assignation in autonomous mode

Mode	DMA and memory transfers	Autonomous peripherals
Stop0 and Stop1 modes	• GPDMA1 and SRAM1 • GPDMA1 and SRAM2 • GPDMA1 and SRAM3 • GPDMA1 and SRAM4	• LPTIM2 • USARTx (x = 1 to 5) • SPI1, SPI2 • I2C1, I2C2, I2C4 • MDF1
Stop0, Stop1 and Stop 2 modes	LPDMA1 and SRAM4 (peripherals on the SRD are listed in the 'Autonomous peripherals' table in the product reference manual)	• ADC4 • DAC1 • LPTIM1, LPTIM3 • LPUART1 • SPI3 • I2C3 • ADF1

6.7.5 PWR security and privilege

The STM32U575/585 embed the same TrustZone security features than the STM32L5. The PWR_SECCFGR register defines whether secure protection is enabled or disabled for the following::

- Low-power mode
- Wake-up (WKUP) pins
- Voltage detection and monitoring
- VBAT mode
- The system clock selection is secure in RCC: the voltage scaling (VOS) configuration and the regulator booster (BOOSTEN) are secure.
- A GPIO is configured as secure: its corresponding bit for pull-up/pull-down configuration in Standby mode is secure.
- The UCPD1 is secure in GTZC. The PWR_UCPDR register is secure.

The STM32U575/585 embed a configuration bit for privileged secure accesses distinct from privileged non-secure ones, in order to define secure privileged and non-secure privileged zones. The table below summarizes the different privilege modes of STM32U575/585 and STM32L5.

Table 46. Privilege modes in STM32L5 and STM32U575/585

STM32L5		STM32U575/585
PWR unprivileged (PRIV = 0 in PWR_PRIVCFGR)	PWR privileged (PRIV = 1 in PWR_PRIVCFGR)	**Secure privileged accesses** (SPRIV = 1 in PWR_PRIVCFGR) This bit can be written by **secure** privileged access only.
Privileged accesses to all PWR registers		Privileged access of all PWR secure functions.
Unprivileged accesses to all PWR registers	Not possible: Unprivileged access to PWR registers is RAZ/WI.	• PWR secure bits can be written only with privileged access, including PWR_SECCFGR. • PWR secure bits can be read only with privileged access. • PWR_SECCFGR and PWR_PRIVCFGR can be read by privileged or unprivileged access. • An unprivileged access to a privileged PWR function is discarded: Read as zero and write is ignored (RAZ/WI).
N/A		**non-secure privileged accesses** (NSPRIV = 1 in PWR_PRIVCFGR) This bit can be written by privileged access only, secure or non-secure. This bit defines the privileged access of all PWR non-secure functions (securable functions that are defined as non-secure).
		• PWR (securable) bits that are configured as non-secure, can be written only with privileged access. • PWR (securable) bits that are configured as non-secure, can be read only with privileged access, except PWR_PRIVCFGR that can be read by privileged or unprivileged accesses. • An unprivileged access to a privileged PWR bit or register is discarded: read as zero and write is ignored (RAZ/WI).

6.7.6 PWR interrupts

The power interrupts sources of STM32L5 and STM32U575/585 are listed in the table below.

Table 47. PWR interrupt sources of STM32L5 and STM32U575/585

Interrupt vector	Description	Event flag	STM32L5	STM32U575/585
PWR_S3WU	Wakeup from Stop 3 interrupt	WUFx (x = 1 to 8)	N/A	24 pins
PVD_PVM	Programmable voltage detector	PVDO	Same	
	USB supply voltage monitor	VDDUSBRDY	EXTI line 35	EXTI line 19
	VDDIO2 supply voltage monitor	VDDIO2RDY	EXTI line 36	EXTI line 20
	Analog supply voltage monitor1	VDDA1RDY	EXTI line 37	EXTI line 21
	Analog supply voltage monitor2	VDDA2RDY	EXTI line 38	EXTI line 22

6.8 CRC

The CRC architecture is the same in STM32U575/585 and STM32L5, with the same features.

7 Migration of timer peripherals

The STM32U575/585 and STM32L5 devices include two advanced-control timers, up to seven general-purpose timers, two basic timers, up to four low-power timers, two watchdog timers and two SysTick timers.

This section compares the features of the above listed timers and RTC in STM32L5 and STM32U575/585 devices.

7.1 Advanced-control timers (TIM1/8)

The STM32U575/585 and STM32L5 include two advanced-control timers, TIM1 and TIM8, with identical features detailed in the table below.

Table 48. Advanced-control timers (TIM1/TIM8) in STM32L5 and STM32U575/585

Feature	STM32U575/585
Counter resolution and type	16-bit up, down, up/down auto-reload counter
Prescaler factor	16-bit programmable prescaler used to divide (also on-the-fly) the counter clock frequency by any factor between 1 and 65536
Channels	Up to six independent channels for: • Input capture (but channels 5 and 6) • Output compare • PWM generation (edge and center-aligned mode) • One-pulse mode output
Complementary outputs	Complementary outputs with programmable dead-time
Synchronization with external circuits and general-purpose timers	Synchronization circuit to control the timer with external signals and to interconnect several timers together The advanced-control (TIM1/TIM8) and general-purpose (TIMx) timers are completely independent, and do not share any resources.
Repetition counter	Repetition counter to update the timer registers only after a given number of counter cycles
Break inputs	Two break inputs to put the timer output signals in a safe user selectable configuration
Interrupt/DMA generation	Interrupt/DMA generation on the following events: • Update: counter overflow/underflow, counter initialization (by software or internal/external trigger) • Trigger event (counter start, stop, initialization or count by internal/external trigger) • Input capture • Output compare
Encoders and sensors	Support incremental (quadrature) encoder and Hall-sensor circuitry for positioning purposes
Trigger input	Trigger input for external clock or cycle-by-cycle current management
Application examples	• Measuring the pulse lengths of input signals (input capture) • Generating output waveforms (output compare, PWM, complementary PWM with dead-time insertion)

The STM32U575/585 and STM32L5 alternate functions (AF) pins of advanced timers TIM1 and TIM8 are mapped as described in the table below.

Table 49. TIM1/8 AF pins on STM32L5 and STM32U575/585

AF pin	STM32L5	STM32U575/585
TIM1_BKIN	PA6	
TIM1_BKIN	PB12	
TIM1_BKIN	PE15	
TIM1_BKIN2	PA11	
TIM1_BKIN2	PE14	
TIM8_BKIN	PA6	
TIM8_BKIN	N/A	PI4
TIM8_BKIN	PB7	
TIM8_BKIN2	PB6	
TIM8_BKIN2	PC9	
TIM1_ETR	PA12	
TIM1_ETR	PE7	
TIM8_ETR	PA0	
TIM8_ETR	N/A	PI13
TIM1_CH1	PA8, PE9	
TIM1_CH1N	PA7, PB13, PE8	PA7, PE8
TIM1_CH2	PA9, PE11	
TIM1_CH2N	PB0, PE10, PB14	
TIM1_CH3	PA10, PE13	
TIM1_CH3N	PB1, PB15, PE12	
TIM1_CH4	PA11, PE14	PA11, PE14
TIM1_CH4N	N/A	PC5, PE15
TIM8_CH1	PC6	PC6, PI5
TIM8_CH1N	PA5, PA7	PA5, PA7, PH13
TIM8_CH2	PC7	PC7, PI6
TIM8_CH2N	PB0, PB14	PB0, PB14, PH14
TIM8_CH2N	PB0, PB14	PB0, PB14, PH14
TIM8_CH3	PC8	PC8, PI7
TIM8_CH3N	PB1, PB15	PB1, PB15, PH15
TIM8_CH4	PC9	PC9, PI2
TIM8_CH4N	N/A	PB2, PD0, PH12

7.2 GP timers with up, down, up-down auto-reload counter (TIM2/3/4/5)

The GP (general-purpose) timers consist of a 16-bit or 32-bit auto-reload counter driven by a programmable prescaler. The STM32U575/585 and STM32L5 devices include GP timers with up, down or up-down auto-reload counter (TIM2, TIM3, TIM4 and TIM5), with identical features detailed in the table below.

Table 50. GP timers with up, down, up-down auto-reload counter in STM32L5 and STM32U575/585

Feature	STM32L5	STM32U575/585
32-bit resolution	TIM2/TIM5	TIM2/TIM3/TIM4/TIM5
16-bit resolution	TIM3, TIM4	-
Counter resolution and type	16- or 32-bit up, down, up/down auto-reload counter	
Prescaler factor	16-bit programmable prescaler used to divide (also on-the-fly) the counter clock frequency by any factor between 1 and 65536	
Channels	Up to four independent channels for: • Input capture • Output compare • PWM generation (edge and center-aligned mode) • One-pulse mode output	
Synchronization with external circuits and other timers	Synchronization circuit to control the timer with external signals and to interconnect several timers	
Interrupt/DMA generation	Interrupt/DMA generation on the following events: • Update: counter overflow/underflow, counter initialization (by software or internal/external trigger) • Trigger event (counter start, stop, initialization or count by internal/external trigger) • Input capture • Output compare	
Encoders and sensors	Supports incremental (quadrature) encoder and Hall-sensor circuitry for positioning purposes	
Trigger input	Trigger input for external clock or cycle-by-cycle current management	
Application examples	• Measuring the pulse lengths of input signals (input capture) • Generating output waveforms (output compare, PWM, complementary PWM with dead-time insertion)	

The STM32U575/585 and STM32L5 AF pins of GP timers TIM2/3/4/5 are mapped as described in the table below.

Table 51. TIM2/3/4/5 AF pins on STM32L5 and STM32U575/585

AF pin	STM32L5	STM32U575/585
TIM2_ETR	PA0, PA5, PA15	
TIM3_ETR	PD2, PE2	
TIM4_ETR	PE0	
TIM5_ETR	PF6	
TIM2_CH1	PA0, PA5, PA15	
TIM2_CH2	PA1, PB3	
TIM2_CH3	PA2, PB10	
TIM2_CH4	PA3, PB11	
TIM3_CH1	PA6, PB4, PC6, PE3	

AF pin	STM32L5	STM32U575/585
TIM3_CH2	PA7, PB5, PC7, PE4	
TIM3_CH3	PB0, PC8, PE5	
TIM3_CH4	PB1, PE6, PC9	
TIM4_CH1	PD12, PB6	
TIM4_CH2	PB7, PD13	
TIM4_CH3	PB8, PD14	
TIM4_CH4	PB9, PD15	
TIM5_CH1	PA0, PF6	PA0, PF6, PH10
TIM5_CH2	PA1, PF7	PA1, PF7, PH11
TIM5_CH3	PA2, PF8	PA2, PF8, PH12
TIM5_CH4	PA3, PF9	PA3, PF9, PI10

7.3 GP timers with auto-reload up-counter (TIM15/16/17)

The STM32U575/585 and STM32L5 devices include three 16-bit resolution GP timers with a 16-bit auto-reload up-counter (TIM15, TIM16 and TIM17) with identical features detailed in the tables below.

Table 52. GP timer with auto-reload up-counter (TIM15) in STM32L5 and STM32U575/585

Feature	STM32L5	STM32U575/585
Counter resolution and type	16-bit auto-reload up-counter	
Prescaler factor	16-bit programmable prescaler used to divide (also on-the-fly) the counter clock frequency by any factor between 1 and 65536	
Channels	Up to two independent channels for: • Input capture • Output compare • PWM generation (edge and center-aligned mode) • One-pulse mode output	
Complementary outputs	Complementary outputs with programmable dead-time (for channel 1 only)	
Synchronization with external circuits and other timers	Synchronization circuit to control the timer with external signals and to interconnect several timers	
Repetition counter	Repetition counter to update the timer registers only after a given number of counter cycles	
Break inputs	One break input to put the timer output signals in the reset state or a known state	
Interrupt/DMA generation	Interrupt/DMA generation on the following events: • Update: counter overflow/underflow, counter initialization (by software or internal/external trigger) • Trigger event (counter start, stop, initialization or count by internal/external trigger) • Input capture • Output compare • Break input (interrupt request)	
Application examples	• Measuring the pulse lengths of input signals (input capture) • Generating output waveforms (output compare, PWM, complementary PWM with dead-time insertion)	

Table 53. GP timers with auto-reload up-counter (TIM16/17) in STM32L5 and STM32U575/585

Feature	STM32L5	STM32U575/585
Counter resolution and type	16-bit auto-reload up-counter	
Prescaler factor	16-bit programmable prescaler used to divide (also on-the-fly) the counter clock frequency by any factor between 1 and 65536	
Channels	Up to two independent channels for: • Input capture • Output compare • PWM generation (edge and center-aligned mode) • One-pulse mode output	
Complementary outputs	Complementary outputs with programmable dead-time (for channel 1 only)	
Repetition counter	Repetition counter to update the timer registers only after a given number of counter cycles	
Break inputs	One break input to put the timer output signals in the reset state or a known state	
Interrupt/DMA generation	Interrupt/DMA generation on the following events: • Update: counter overflow/underflow, counter initialization (by software or internal/external trigger) • Trigger event (counter start, stop, initialization or count by internal/external trigger) • Input capture • Output compare • Break input (interrupt request)	
Application examples	• Measuring the pulse lengths of input signals (input capture) • Generating output waveforms (output compare, PWM, complementary PWM with dead-time insertion)	

The STM32U575/585 and STM32L5 AF pins of GP timers TIM15/16/17 are mapped as described in the table below.

Table 54. TIM15/16/17 AF pins on STM32L5 and STM32U575/585

AF pin	STM32L5	STM32U575/585
TIM15_BKIN	PA9, PB12	
TIM16_BKIN	PB5	
TIM17_BKIN	PA10, PB4	
TIM15_CH1	PA2, PB14, PF9, PG10	
TIM15_CH1N	PA1, PB13, PG9	
TIM15_CH2	PA3, PB15, PF10, PG11	
TIM16_CH1	PA6, PB8, PE0	
TIM16_CH1N	PB6	
TIM17_CH1	PA7, PB9, PE1	
TIM17_CH1N	PB7	

7.4 Basic timers (TIM6/7)

The basic timers TIM6 and TIM7 consist in a 16-bit auto-reload counter driven by a programmable prescaler. These timers are completely independent, and do not share any resources. The STM32U575/585 and STM32L5 devices have the same basic timers features detailed in the table below.

Table 55. Basic timers (TIM6/TIM7) in STM32L5 and STM32U575/585

Feature	STM32L5	STM32U575/585
Counter resolution and type	16-bit auto-reload up-counter	
Prescaler factor	16-bit programmable prescaler used to divide (also on-the-fly) the counter clock frequency by any factor between 1 and 65536	
Synchronization signals	Synchronization circuit to trigger the DAC	
Interrupt/DMA generation	Interrupt/DMA generation on the update event, counter overflow	
Application examples	• Time-base generation • Driving the DAC	

The basic timers TIM6 and TIM7 have no AF pins mapped to I/O, on both STM32L5 and STM32U575/585.

7.5 Low-power timers (LPTIM1/2/3/4)

The LPTIMx is a 16-bit timer that benefits from the ultimate developments in power-consumption reduction. The STM32U575/585 include four LPTIMs versus three in the STM32L5. LPTIMs share the same features in both series, but new features are added in STM32U575/585 such as:

- Two independent channels per LPTIM
- Input capture channel
- DMA requests
- Autonomous function in Stop modes

The table below summarizes the LPTIMx features in STM32L5 and STM32U575/585.

Table 56. LPTIMx in STM32L5 and STM32U575/585

Feature	STM32L5	STM32U575/585
LPTIMx	LPTIM1, LPTIM2 and LPTIM3	LPTIM1, LPTIM2, LPTIM3 and LPTIM4
Counter resolution and type	16 bit up-counter	
Prescaler factor	3-bit prescaler with eight possible dividing factors (1, 2, 4, 8, 16, 32, 64 or 128)	
Selectable clock	• Internal clock sources: LSE, LSI, HSI or APB clock • External clock source over LPTIM input (working with no LP oscillator running, used by pulse counter application)	
Auto-reload	16-bit ARR auto-reload register	
Capture/compare	16-bit capture/compare register	
Continuous mode	Continuous/One-shot mode	
Trigger mode	Selectable software/hardware input trigger	
Glitch filter	Programmable digital glitch filter	
Configurable output	Configurable output: pulse, PWM	
Polarity	Configurable I/O polarity	
Encoder mode	Encoder mode	
Repetition counter	Repetition counter to update the timer registers only after a given number of counter cycles	

Feature	STM32L5	STM32U575/585
Input capture, PWM and one-pulse channels	N/A	Up to two independent channels for: • Input capture • PWM generation (edge and center-aligned mode) • One-pulse mode output
Interrupt generation on events	9 events	10 events
DMA requests	N/A	DMA request generation on the following events: • Update event • Input capture

The above features are not similarly implemented on LPTIMs peripherals, as described in the table below.

Table 57. LPTIMx feature implementation in STM32L5 and STM32U575/585

Feature	STM32L5			STM32U575/585			
	LPTIM1	LPTIM2	LPTIM3	LPTIM1	LPTIM2	LPTIM3	LPTIM4
Encoder mode	X	-	-	X	X	-	-
PWM mode	X	X	X	X	X	X	X
Input Capture	-	-	-	X	X	X	-
Number of channels	1	1	1	2	2	2	-
Number of DMA requests	-	-	-	3	3	3	-
Wakeup from Stop mode	X(1)	X(2)	X(1)	X(1)	X(2)	X(1)	X(1)
Autonomous mode	-	-	-	X	X	X	-

1. *Wakeup supported from Stop 0, Stop 1 and Stop 2 modes.*
2. *Wakeup supported from Stop 0 and Stop 1 modes.*

The STM32U575/585 and STM32L5 AF pins of LP timers LPTIM1/2/3 and LPTIM4 (only in STM32U575/585) are mapped as described in the table below.

Table 58. LPTIMx AF pins on STM32L5 and STM32U575/585

AF pin	STM32L5	STM32U575/585
LPTIM1_ETR	PB6, PC3, PG12	
LPTIM2_ETR	PA5, PC3, PD11	
LPTIM3_ETR	PB14, PC10, PF4	PB14, PC10, PD10, PF4
LPTIM4_ETR	N/A	PD2, PF12
LPTIM1_CH1		PA14, PB2, PB3, PC1, PG15
LPTIM1_CH2		PA1, PB4, PG14
LPTIM2_CH1		PA4, PA8, PD13
LPTIM2_CH2		PA7, PC7, PD10
LPTIM3_CH1		PB0, PB10, PC3, PC8, PF5
LPTIM3_CH2		PB1, PC9, PD15, PF2
LPTIM4_CH1		N/A
LPTIM4_CH2		
LPTIM1_IN1	PB5, PC0, PG10	

AF pin	STM32L5	STM32U575/585
LPTIM1_IN2	PB7, PC2, PG11	
LPTIM1_OUT	PA14, PB2, PC1, PG15	N/A
LPTIM2_IN1	PB1, PC0, PD12	
LPTIM2_IN2	N/A	PA10, PB15, PD9
LPTIM2_OUT	PA4, PA8, PD13	N/A
LPTIM3_IN1	PB13, PC11, PF3	PB13, PC11, PF3, PD9
LPTIM3_IN2	N/A	
LPTIM3_OUT	PB10, PC3, PF5	N/A
LPTIM4_IN1	N/A	PD13, PF11
LPTIM4_IN2		N/A
LPTIM4_OUT		PD7, PF13

7.6 Watchdogs

The STM32U575/585 and STM32L5 devices embed two watchdogs:

- a system window watchdog (WWDG) with same features
- an independent watchdog (IWDG) with same features except the STM32U5 capability to generate an early wakeup interrupt

Table 59. IWDG features in STM32L5 and STM32U575/585

Feature	STM32L5	STM32U575/585
LSI used as IWDG kernel clock (iwdg_ker_ck)	X	X
Window function	X	X
Early wakeup interrupt generation	-	X
System reset generation (refer to the RCC section of the product reference manual for more details)	X	X
Capability to work in system Stop	X	X
Capability to work in system Standby	X	X
Capability to generate an interrupt in system Stop	-	X
Capability to generate an interrupt in system Standby	X	X
Capability to be frozen when the MCU enters in debug mode	X	X
Option bytes to control the activity in Stop mode	-	X
Option bytes to control the activity in Standby mode	-	X
Option bytes to control the hardware mode	-	X

7.7 Real-time clock (RTC)

The STM32U575/585 devices implement the same RTC features than the STM32L5, but with the introduction of the new binary mode with 32-bit free-running counter (refer to the product reference manual for more details).

The STM32U575/585 and STM32L5 AF pins of RTC are mapped as described in the table below.

Table 60. RTC AF pins in STM32L5 and STM32U575/585

AF pin	STM32L5	STM32U575/585
RTC_REFIN	PB15	
RTC_TS	PC13	
RTC _OUT1	PC13	
RTC _OUT2	PB2	

7.8 SysTick timer

The STM32U575/585 and STM32L5 Cortex-M33 with TrustZone embeds two SysTick timers. When TrustZone is activated, the two SysTick timers are available, but when TrustZone is disabled, only one SysTick timer is available.

This SysTick timer (secure or non-secure) is dedicated to real-time operating systems, but can also be used as a standard down-counter.

8 Migration of communication peripherals

8.1 Serial peripheral interface (SPI)

This section highlights the SPI features implemented on STM32L5 and STM32U575/585 devices.

Both families share the same SPI features. What is new in the STM32U575/585 is the autonomous mode, new slave selects (SS) features pin signal, new ready (RDY) signal and separation of clock domains into three independent domains.

Table 61. SPI features in STM32L5 and STM32U575/585

Feature	STM32L5	STM32U575/585
SPI peripherals	SPI1, SPI2 and SPI3 (same features in the three instances)	• SPI1, SPI2 (full feature set instances) • SPI3 (limited feature set instance)
Full-duplex synchronous transfer on three lines	X	X
Half-duplex synchronous transfer on two lines (with bidirectional data line)	X	X
Simplex synchronous transfer on two lines (with unidirectional data line)	X	X
Data size	4- to 16-bit data size selection	4- to 32-bit data size selection on SPI1, SPI2
	N/A	Fixed to 8- and 16-bit only on SPI3
Multimaster or multislave mode capability	X	X
Clock inputs	One input: PCLK is the unique SPI clock source.	Two independent clock inputs: peripheral kernel clock (spi_ker_ck) is independent of PCLK.
Baudrate prescalers	Master/slave mode baudrate prescalers up to f_{PCLK} / 2	Baudrate prescaler up to kernel frequency / 2
	N/A	spi_ker_ck prescaler can be bypassed from RCC in master mode.
Protection of configuration and settings	N/A	X
Slave select (SS) management	NSS management by hardware or software for both master and slave: dynamic change of master/slave operations	Hardware or software management of SS for both master and slave
Adjustable minimum delays between data and between SS and data flow	N/A (fixed)	X
Configurable SS signal polarity and timing	N/A	Configurable SS signal polarity and timing, MISO x MOSI swap capability
Programmable clock polarity and phase	X	X
Programmable data order with MSB-first or LSB-first shifting	X	X
Programmable transaction data	X	Programmable number of data within a transaction to control SS and CRC
Dedicated transmission and reception flags with interrupt capability	X	X
SPI Motorola and Texas Instrument formats support	X	X

Feature	STM32L5	STM32U575/585
Hardware CRC feature can secure communication at the end of transaction by: • adding CRC value in Tx mode • automatic CRC error checking for Rx mode	CRC fixed to 8- or 16-bit for all SPIs	• SPI1 and SPI2: CRC polynomial length configurable from 9 to 17 bits • SPI3: CRC polynomial length configurable from 9 to 17 bits
Interrupt events and error detection with interrupt capability	Interrupts: • Transmit TXFIFO ready to be loaded • Data received in receive RXFIFO • Master mode fault • Overrun error • TI frame format error • CRC protocol error	Interrupts: • TxFIFO ready to be loaded • Data received in RxFIFO • Both TXP and RXP active • Transmission Transfer Filled • Overrun error • Underrun error • TI frame format Error • CRC error • Mode fault • End of transfer • Master mode suspended • TxFIFO transmission complete
	N/A	All the interrupt events can wak eup the system from Sleep mode at each instance
FIFO size	Two 32-bit embedded Rx and Tx FIFOs with DMA capability	Two 16x or 8x 8-bit embedded Rx and TxFIFOs with DMA capability
Number of transferred data	Number defined by the counter for the SPI transmission DMA channel	Programmable number of data in transaction: • SPI1 and SPI2: unlimited, expandable • SPI3: up to 1024 (no data counter)
FIFO thresholds	Fixed threshold to 1/2 FIFO or 1/4 FIFO level	Configurable FIFO thresholds (data packing)
Configurable behavior at slave underrun condition	N/A	X (support of cascaded circular buffers)
Autonomous functionality in Stop modes (handling of the transaction flow and required clock distribution) with wakeup from Stop capability	N/A	• SPI 1/2: Stop 0 and Stop 1 modes with wakeup • SPI3: Stop 0, Stop 1 and Stop 2 modes
RDY status pin	N/A	Optional status pin RDY signalizing the slave device ready to handle the data flow

8.1.1 Mapping of SPI alternate function pins

In STM32U575/585 and STM32L5 devices, SPI peripherals have the same mapping of alternate function (AF) pins: SPIx_SCK, SPIx_NSS, SPIx_MISO and SPIx_MOSI AF pins (x = 1 to 3) are fully compatible. However, the STM32U575/585 packages have a new AF pin called SPIx_RDY (x = 1 to 3), not present in STM32L5.

Table 62. SPIx_RDY AF pins in STM32L5 and STM32U575/585

AF pin function	STM32L5	STM32U575/585
SPI1_MOSI	PA7, PE15, PG4, PA12, PB5	
SPI1_MISO	PA6, PE14, PG3, PA11, PB4	
SPI1_SCK	PA1, PA5, PE13, PG2, PB3	
SPI1_NSS	PA4, PB0, PE12, PG5, PA15	
SPI1_RDY	N/A	PA8, PB2, PE11, PG6, PA2
SPI2_MOSI	PC1, PC3, PB15, PD4	
	N/A	PI3
SPI2_MISO	PC2, PB14, PD3	
	N/A	PI2
SPI2_SCK	PB13, PA9, PD3, PD1, PB10	
	N/A	PI1
SPI2_NSS	PB12, PD0, PB9	
	N/A	PI0
SPI2_RDY	N/A	PB11, PC0, PD5, PI4
SPI3_MOSI	PC12, PD6, PG11, PB5	
SPI3_MISO	PC11, PG10, PB4	
SPI3_SCK	PC10, PG9, PB3	
SPI3_NSS	PA4, PA15, PG12	
SPI3_RDY	N/A	PA0, PB8, PG13

The slave select (SS) and ready (RDY) signals can be applied optionally just to set up the communication with concrete slave and to assure the data flow is properly handled. The Motorola® data format is used by default, but some other specific modes are supported as well. The main features of SPI_RDY pin implementation are the following:

- In master, the RDY input stops the communication acting on the MFSM. This requires some clock cycles due to synchronizers.
- Slave puts the RDY pin low when TXFIFO is almost empty or RXFIFO is almost full, to be able to stop master even if there is a free location on FIFOs. This is not true (RDY pin remains high) when the communication is at the end.
- RDY feature cannot be used when the data size is configured shorter than 8 bits.

8.1.2 SPI autonomous mode

The three SPI peripherals in STM32U575/585 support autonomous operation down to Stop mode with the following main features:

- The SPI can handle and initialize transactions autonomously, requiring no specific system execution interaction till the ongoing transaction ends.
- SPI logic is able to provide temporary clock requests addressed to RCC to ensure clocking of those SPI domains just necessary for handling the data flow with SRAM.
- In Stop mode, the APB clock is requested by the peripheral each time the SPI registers need to be updated, based on specific traffic events (mainly TXP and RXP).
- Slave mode: Kernel requests are generated only for TI mode in order to have the delay on MISO.
- Master mode: The SCK signal is derived from the kernel clock fed from RCC upon permanent kernel clock request, provided by the SPI when the device is in Stop mode.

8.2 I2C

The STM32U575/585 I2C peripherals share the same feature as the STM32L5 ones. Differences between STM32L5 and STM32U575/585 I2C are shown in the table below.

In addition, the STM32U575/585 I2C embed the autonomous mode of I2C peripherals, allowing the I2C to be functional in Stop mode. The I2C receives its kernel clock only when it is implicated in the transfer. It is possible also to use the autonomous mode in Run, Sleep or Stop modes.

Table 63. I2C features in STM32L5 and STM32U575/585

Feature	STM32L5	STM32U575/585
Number of instances	I2C1, I2C2, I2C3, I2C4	
7- and 10-bit addressing mode		
Standard-mode (up to 100 Kbit/s)		
Fast-mode (up to 400 Kbit/s)		
Fast-mode Plus with 20mA output drive I/Os (up to 1 Mbit/s)		
Independent clock		
SMBus/PMBus™		
Wakeup from Stop 0 and Stop 1 modes		
Wakeup from Stop 2 mode	I2C3	
Autonomous mode	N/A	I2C1, I2C2 and I2C4 in CD (CPU domain) I2C3 in SRD (SmartRun domain)

The table below summarizes the I2C AF pinout compatibility between STM32L5 and STM32U575/585.

Table 64. I2C AF pins in STM32L5 and STM32U575/585

AF pin function	STM32L5	STM32U575/585
I2C1_SCL	PB6, PB8, PG14	
I2C1_SDA	PB7, PB9, PG13	
	N/A	PB3
I2C1_SMBA	PA1, PA14, PB5, PG15	
I2C2_SCL	PB10, PB13, PF1	
	N/A	PH4
I2C2_SDA	PB11, PB14, PF0	

AF pin function	STM32L5	STM32U575/585
I2C2_SDA	N/A	PH5
I2C2_SMBA	PB12, PF2	
	N/A	PH6
I2C3_SCL	PA7, PC0, PG7, PH7	
I2C3_SDA	PB4, PC1, PG8	
	N/A	PH8
I2C3_SMBA	PB2, PG6	
	N/A	PH9
I2C4_SCL	PB6, PB10, PD12, PF14	
I2C4_SDA	PB7, PB11, PD13, PF15	
I2C4_SMBA	PA14, PD11, PF13	

8.3 U(S)ART and LPUART

The STM32U575/585 devices implement the same U(S)ART (universal synchronous asynchronous receiver transmitter) and LPUART (low-power UART) features than the STM32L5, with three USARTs, two UARTs and one LPUART. The STM32U575/585 LPUART has a new feature, the autonomous mode that allows LPUART to be functional in Stop mode. This autonomous mode can be used in Run, Stop and Sleep modes (refer to the product reference manual for more details).

Table 65. U(S)ART/LPUART features in STM32L5 and STM32U575/585

Feature	STM32L5	STM32U575/585
Number of instances	USART1, USART2, USART3, UART4, UART5	
Interrupts	23 interrupt sources with flag	
Hardware flow control for modem	X	
Continuous communication using DMA	X	
Multiprocessor communication	X	
Synchronous mode (master/slave)	USART1, USART2, USART3	
Smartcard mode		
Single-wire half-duplex communication	X	
IrDA SIR ENDEC block	All except LPUART	
LIN mode		
Dual-clock domain and wakeup from Stop mode	All except LPUART support wakeup from Stop 0 and Stop 1 modes. LPUART supports wakeup from Stop 0, Stop 1 and Stop 2 modes.	
Receiver timeout interrupt	All except LPUART	
Modbus communication		
Auto-baudrate detection		
LPUART limitation	LPUART does not support Synchronous mode (SPI master), Smartcard mode, IrDA, LIN, Modbus, receiver timeout interrupt and auto-baudrate detection.	
Driver enable	X	
USART data length	7, 8 and 9 bits	
Tx/Rx FIFO	X	

Feature	STM32L5	STM32U575/585
Tx/Rx FIFO size	8 bits	
Autonomous mode	-	X

The AF pins of these peripherals are fully compatible in STM32L5 and STM32U575/585 similar packages. STM32U575/585 and STM32L5 AF pins of UART/USART and LPUART instances are mapped as described in the table below.

Table 66. U(S)ART/LPUART AF pins in STM32L5 and STM32U575/585

AF pin function	STM32L5	STM32U575/585
USART1_TX	PA9, PB6, PG9	
USART1_RX	PA10, PB7, PG10	
USART1_CK	PA8, PB5, PG13	
USART1_CTS	PA11, PB4, PG11	
USART1_RTS_DE	PA12, PB3, PG12	
USART2_TX	PA2, PD5	
USART2_RX	PA3, PA15, PD6	
USART2_CK	PA4, PD7	
USART2_CTS	PA0, PD3	
USART2_RTS_DE	PA1, PD4	
USART3_TX	PB10, PC4, PC10, PD8	
	N/A	PA7
USART3_RX	PB11, PC5, PC11, PD9	
	N/A	PA5
USART3_CK	PB0, PB12, PC12, PD10	
USART3_CTS	PA6, PB13, PD11	
USART3_RTS_DE	PA15, PB1, PB14, PD2, PD12	
USART4_TX	PA0, PC10	
USART4_RX	PA1, PC11	
USART4_CK	N/A	
USART4_CTS	PB7	
USART4_RTS_DE	PA15	
USART5_TX	PC12	
USART5_RX	PD2	
USART5_CK	N/A	
USART5_CTS	PB5	
USART5_RTS_DE	PB4	
LPUART1_TX	PA2, PB11, PC1, PG7	
LPUART1_RX	PA3, PB10, PC0, PG8	
LPUART1_CK	N/A	
LPUART1_CTS	PA6, PB13, PG5	
LPUART1_RTS_DE	PB1, PB12, PG6	

8.4 Serial-audio interface (SAI)

The SAI offers a wide set of audio protocols due to its flexibility and wide range of configurations. Many stereo or mono audio applications may be targeted. I^2S standards, LSB- or MSB-justified, PCM/DSP, TDM, and AC'97 protocols may be addressed for example. SPDIF output is offered when the audio block is configured as a transmitter.

The STM32U575/585 or STM32L5 devices embed two SAI, SAI1 and SAI2, with exactly the same features as described in the table below.

Table 67. SAI features in STM32L5 and STM32U575/585

Feature	STM32L5 and STM32U575/585	
	SAI1	SAI2
I^2S standards, LSB- or MSB-justified, PCM/DSP, TDM, and AC'97 protocols	X	
Mute mode		
Stereo and mono audio frame capability		
Configurable data size (8, 10, 16, 20, 24, or 32 bits)		
SPDIF		
FIFO size	8 words	
PDM	X	-

The SAI1 and SAI2 pins/balls are fully compatible except that SAI2_EXTCLK pin is not mapped in STM32U575/585 packages.

The AF pins of these peripherals are fully compatible in STM32L5 and STM32U575/585 similar packages. STM32U575/585 and STM32L5 AF pins of SAI instances are mapped as described in the table below.

Table 68. SAI AF pins in STM32L5 and STM32U575/585

AF pin function	STM32L5	STM32U575/585
SAI1_CK1	PA3, PB8, PE2, PG7	
SAI1_CK2	PA8, PE5	
SAI1_SCK_A	PA8, PB10, PE5	
SAI1_SCK_B	PB3, PE8, PF8	
SAI1_SD_A	PA10, PC1, PC3, PD6, PE6	
SAI1_SD_B	PA13, PB5, PE3, PE7, PF6	
SAI1_FS_A	PA9, PB9, PE4	
SAI1_FS_B	PA4, PA14, PB6, PE9, PF9	
SAI1_D1	PA10, PC3, PD6, PE6	
SAI1_D2	PB9, PE4	
SAI1_D3	PC5, PF10	
SAI1_MCLK_A	PA3, PB8, PE2, PG7	
SAI1_MCLK_B	PB4, PE10, PF7	
SAI1_EXTCLK(1)/ AUDIOCLK(2)	PA0, PB0	
SAI2_SCK_A	PB13, PD10, PG9	
SAI2_SCK_B	PC10, PG2	
SAI2_SD_A	PB15, PD11, PG12	

AF pin function	STM32L5	STM32U575/585
SAI2_SD_B	PC12, PG5	
SAI2_FS_A	PB12, PC0, PD12, PG10	
SAI2_FS_B	PA15, PG3	
SAI2_MCLK_A	PB14, PC6, PD9, PG11	
SAI2_MCLK_B	PC7, PC11, PG4	
SAI2_EXTCLK	PA2, PC9	N/A

1. *On STM32L5.*
2. *On STM32U575/585.*

8.5 FD controller area network (FDCAN)

The controller area network (CAN) subsystem consists of one CAN module, a shared message RAM memory and a configuration block.

The modules (FDCAN) are compliant with ISO 11898-1: 2015 (CAN protocol specification version 2.0 part A, B) and CAN FD protocol specification version 1.0. A 0.8-Kbyte message RAM implements filters, receives FIFOs, transmits event FIFOs and transmits FIFOs.

The STM32U575/585 and STM32L5 devices embed one FDCAN peripheral with exactly the same features as listed in the table below.

Table 69. FDCAN features in STM32L5 and STM32U575/585

Feature	STM32L5 and STM32U575/585
Number of instances	FDCAN1
Number of interrupts	2
Conform with CAN protocol version 2.0 part A, B and ISO 11898-1: 2015, -4	X
CAN FD with maximum 64 data bytes supported	
CAN error logging	
AUTOSAR and J1939 support	
Improved acceptance filtering	
Two receive FIFOs of three payloads each (up to 64 bytes per payload)	
Separate signaling on reception of high-priority messages	
Configurable transmit FIFO/queue of three payload (up to 64 bytes per payload)	
Configurable transmit event FIFO	
Programmable loop-back test mode	
Maskable module interrupts	
Two clock domains: APB bus interface and CAN core kernel clock	
Power-down support	

The FDCAN AF pins are fully compatible on similar packages. In addition, STM32U575/585 map FDCAN1_RX and FDCAN1_TX signals on PF7 and PF8 pins respectively. STM32U575/585 and STM32L5 AF pins of FDCAN1 are mapped as described in the table below.

Table 70. FDCAN AF pins in STM32L5 and STM32U575/585

AF pin function	STM32L5	STM32U575/585
FDCAN1_RX	PA11, PB8, PD0	
	N/A	PF7, PH14
FDCAN1_TX	PA12, PB9, PD1	
	N/A	PF8, PH13

8.6 SDMMC

The SD/SDIO MultiMediaCard host interface (SDMMC) provides an interface between the AHB bus and SD memory cards, SDIO cards and MMC devices. The STM32U575/585 embed two SDMMCs with almost the same features as the SDMMC1 in the STM32L5. The internal DMA (IDMA) linked-list, SDR104 and HS200 operating modes are the main new features implemented in STM32U575/585.

Table 71. SDMMC features in STM32L5 and STM32U575/585

Feature	STM32L5	STM32U575/585
Number of instances	SDMMC1	SDMMC1, SDMMC2
Pinout compatibility	SDMMC1 AF pins are fully compatible.	
Compliance with *Embedded MultiMediaCard System*	Specification version 4.51	Specification version 5.1
	Card support for three different data bus modes: 1-bit (default), 4-bit and 8-bit	
	N/A	HS200 SDMMC_CK speed limited to maximum allowed I/O speed, HS400 is not supported.
Backward compatibility	Full compatibility with previous versions of MultiMediaCards	
Compliance with SD memory card specifications	Full compliance with *SD memory card specifications version 4.1*	Full compliance with *SD memory card specifications version 6.0*
	N/A	SDR104 SDMMC_CK speed limited to maximum allowed I/O speed
	SPI mode and UHS-II mode not supported	
Compliance with *SDIO card specification version 4.0*	Full compliance with *SDIO card specification version 4.0.* Card support for two different databus modes: 1-bit (default) and 4-bit.	
	N/A	SDR104 SDMMC_CK speed limited to maximum allowed I/O speed
	SPI mode and UHS-II mode not supported	
Data transfer speed	Up to 104 Mbyte/s for the 8-bit mode, depending on maximum allowed I/O speed	
Control of external bidirectional drivers	Data and command output enable signals to control external bidirectional drivers	
Internal IDMA transfer	The IDMA supports burst transfers of 8 beats, in transmit and receive burst transfer modes.	
Internal IDMA channel configuration	IDMA provides a single-buffered channel configurations.	
	IDMA provides a double-buffered channel configurations.	N/A
	N/A	IDMA provides a linked-list support channel configuration.

Feature	STM32L5	STM32U575/585
Connection to the host	The MultiMediaCard/SD bus connects cards to the host.	
Number of SD cards supported	The SDMMC current version supports only one SD/SDIO/e•MMC™ card at any one time and a stack of e•MMC™.	
SD and SDIO operation modes	DS (default speed), HS (high speed), SDR12, SDR25, DDR50, SDR50 (optional use of variable delay for this latter)	
	N/A	SDR104: This mode requires variable delay support using sampling point tuning. The delay can be provided by delay block (DLYB) peripheral.(1)
e•MMC operation modes	Legacy compatible, high-speed SDR, high-speed DDR	
	N/A	High speed HS200: This mode requires variable delay support using sampling point tuning. The delay can be provided by delay block (DLYB) peripheral.(1)

1. *The DLYB can be used in conjunction with the SDMMC adapter, to tune the phase of the sampling clock for incoming data in SDMMC receive mode. It is required for the SDMMC to support the SDR104 and HS200 operating modes, and it is optional for SDR50 and DDR50 modes.*

STM32U575/585 and STM32L5 AF pins of SDMMC1 are fully compatible and mapped as described in the table below (no SDMMC2 in the STM32L5).

Table 72. SDMMC AF pins in STM32L5 and STM32U575/585

AF pin function	STM32L5	STM32U575/585
SDMMC1_CKIN	PB8	
SDMMC1_CDIR	PB9	
SDMMC1_D0DIR	PC6	
SDMMC1_D123DIR	PC7	
SDMMC1_CK	PC12	
SDMMC1_CMD	PD2	
SDMMC1_D0	PC8	
SDMMC1_D1	PC9	
SDMMC1_D2	PC10	
SDMMC1_D3	PC11	
SDMMC1_D4	PB8	
SDMMC1_D5	PB9, PC0	
SDMMC1_D6	PC6	
SDMMC1_D7	PC7	
SDMMC2_CKIN	N/A	
SDMMC2_CDIR		
SDMMC2_D0DIR		
SDMMC2_D123DIR		
SDMMC2_CK	N/A	PC1, PD6
SDMMC2_CMD		PA0, PD7
SDMMC2_D0		PB14
SDMMC2_D1		PB15
SDMMC2_D2		PB3
SDMMC2_D3		PB4
SDMMC2_D4		PB8
SDMMC2_D5		PB9
SDMMC2_D6		PC6
SDMMC2_D7		PC7

8.7 DCMI and PSSI

The DCMI (digital camera interface) and PSSI (parallel synchronous slave interface) peripherals are present in STM32U575/585 only.

DCMI and PSSI use the same circuitry and cannot then be used at the same time: when using the PSSI, the DCMI registers cannot be accessed, and vice-versa. In addition, PSSI and DCMI share the same alternate functions and interrupt vector.

The DCMI main features are the following:

- 8-, 10-, 12- or 14-bit parallel interface
- Embedded/external line and frame synchronization
- Continuous or snapshot mode
- Crop feature
- Following data formats supported:
  - 8-, 10-, 12-, and 14-bit progressive video (either monochrome or raw Bayer)
  - YCbCr 4:2:2 progressive video
  - RGB 565 progressive video
  - Compressed data JPEG

The PSSI peripheral main features are listed below:

- Slave mode operation
- 8- or 16-bit parallel data input or output
- 4-word (16-byte) FIFO
- Data enable (PSSI_DE) alternate function input and ready (PSSI_RDY) alternate function output

STM32U575/585 AF pins of DCMI and PSSI are mapped as described in the table below (no DCMI and PSSI in STM32L5).

Table 73. DCMI and PSSI AF pins in STM32U575/585

DCMI AF pin function	PSSI AF pin function	STM32U575/585
DCMI_HSYNC	PSSI_DE	PA4, PD8, PH8
DCMI_PIXCLK	PSSI_PDCK	PA6, PD9, PH5
DCMI_VSYNC	PSSI_RDY	PB7, PI5
DCMI_D0	PSSI_D0	PA9, PC6, PH9
DCMI_D1	PSSI_D1	PA10, PC7, PH10
DCMI_D2	PSSI_D2	PC8, PC11, PE0, PH11
DCMI_D3	PSSI_D3	PC9, PE1, PH12
DCMI_D4	PSSI_D4	PC11, PE4, PH14
DCMI_D5	PSSI_D5	PB6, PD3, PI4
DCMI_D6	PSSI_D6	PB8, PE5, PI6
DCMI_D7	PSSI_D7	PB9, PE6, PI7
DCMI_D8	PSSI_D8	PC10, PH6, PI1
DCMI_D9	PSSI_D9	PC12, PH7, PI2
DCMI_D10	PSSI_D10	PB5, PD6, PI3
DCMI_D11	PSSI_D11	PD2, PF10, PH15
DCMI_D12	PSSI_D12	PB4, PF11, PF6
DCMI_D13	PSSI_D13	PG15, PI0

8.8 Universal serial bus interface (USB)

The STM32U575/585 and STM32L5 devices embed one USB Type-C/USB Power Delivery interface (UCPD) with the same features. STM32U575/585 implement one USB OTG_FS (on-the-go full-speed) while the STM32L5 include one USB FS.

All features supported by the STM32L5 are also supported by the STM32U575/585. The later implements also advanced features related to OTG/Host operating modes.

Table 74. USB features in STM32L5 and STM32U575/585

Feature	STM32L5	STM32U575/585
Certification	USB specification version 2.0 full-speed compliant	USB-IF certified to the Universal Serial Bus Specification Rev 2.0
Full support (PHY) for the OTG protocol	N/A	Full support (PHY) for the OTG protocol detailed in the *On-The-Go Supplement Rev 2.0 specification*: • Integrated support for A-B device identification (ID line) • Integrated support for host negotiation protocol (HNP) and session request protocol (SRP) • Allows the host to turn VBUS off to conserve battery power in OTG applications. • Supports OTG monitoring of VBUS levels with internal comparator. • Supports dynamic host-peripheral switch of role.
Software configurable		Software-configurable to operate as: • SRP capable USB FS peripheral (B-device) • SRP capable USB FS/LS host (A-device) • USB OTG_FS dual-role device
FS SOF and LS keep-alive support		Supports FS SOF (start of frame) and LS keep-alive with: • SOF pulse PAD connectivity • SOF pulse internal connection to timer (TIMx) • Configurable framing period • Configurable end-of-frame interrupt
Power saving	USB suspend/resume operations	System stop during USB suspend, switch-off of clock domains internal to the digital core, PHY and DFIFO power management
Dedicated memory	Dedicated packet buffer memory (SRAM) of **1 Kbyte**	Dedicated RAM of **1.25 Kbytes** with advanced FIFO control: • Configurable partitioning of RAM space into different FIFOs for flexible and efficient use of RAM • Each FIFO can hold multiple packets. • Dynamic memory allocation • Configurable FIFO sizes that are not factor of two, to allow the use of contiguous memory locations Guarantees max USB bandwidth for up to one frame (1 ms) without system intervention.
Battery charging	Battery charging specification revision 1.2 support	BCD (battery charging detection) support: It supports charging port detection as described in battery charging specification revision 1.2 on the FS PHY transceiver only.
Other general features	CRC (cyclic redundancy check) generation/ checking, NRZI (non-return-to-zero inverted) encoding/decoding and bit-stuffing	N/A
	Frame-locked clock-pulse generation	
	USB 2.0 LPM (link power management) support	
	USB connect/disconnect capability (controllable embedded pull-up resistor on USB_DP line)	
	N/A	ADP (attach detection protocol) support
Peripheral-mode	N/A	• 1 bidirectional control endpoint0

Feature	STM32L5	STM32U575/585
Peripheral-mode		• 6 device bidirectional endpoints (including EP0)
	8 configurable number of endpoints (EP) to support bulk, interrupt or isochronous transfers: • 4 IN endpoints • 4 OUT endpoints	12 configurable EP (6 IN + 6 OUT, including the control endpoint) to support bulk, interrupt or isochronous transfers: • 5 IN endpoints • 5 OUT endpoints
	Double-buffered bulk/isochronous endpoint support	• Management of a shared Rx FIFO and a Tx-OUT FIFO for efficient usage of the USB data RAM • Management of up to 6 dedicated Tx-IN FIFOs (one for each active IN EP) to put less load on the application • Bidirectional endpoints fully usable in isochronous (or bulk) mode thanks to an advanced FIFO buffer memory management (no double-buffer mode that would reduce the number of available endpoints)
	N/A	Support for the soft disconnect feature
Host mode	N/A	• External charge pump for VBUS voltage generation • Up to 12 host channels (pipes): each channel is dynamically reconfigurable to allocate any type of USB transfer.
		Built-in hardware scheduler holding: • Up to 12 interrupt plus isochronous transfer requests in the periodic hardware queue • Up to 12 control plus bulk transfer requests in the non-periodic hardware queue
		Management of a shared Rx FIFO, a periodic Tx FIFO and a non-periodic Tx FIFO for efficient usage of the USB data RAM

The AF pins of USB peripherals in STM32U575/585 and STM32L5 are not compatible as detailed in the table below.

Table 75. USB AF pins in STM32L5 and STM32U2575/585

AF pin name	Pin number	
	STM32L5	STM32U2575/585
OTG_FS_SOF	N/A	PA8, PA14
OTG_FS_ID		PA10
OTG_FS_DM/USB_DM	PA11	
OTG_FS_DP/USB_DP	PA12	
OTG_FS_NOE	PA13, PC9	
USB_DM	PA11	N/A
USB_DP	PA12	
USB_NOE	PA13, PC9	
UCPD1_DB2	PB14	
UCPD1_CC2	PB15	
UCPD1_CC1	PA15	

AF pin name	Pin number	
	STM32L5	STM32U2575/585
UCPD1_DB1	PB5	
UCPD1_FRSCC1	PA2	
UCPD1_FRSCC1	PB2	
UCPD1_VCONNEN1	N/A	PB6, PB13
UCPD1_VCONNEN2		PB7, PC0
UCPD1_FRSCC2	PB13, PC11, PG6, PG7	

9 Migration of analog peripherals

9.1 Analog-to-digital converter (ADC)

The STM32U575/585 and STM32L5 embed two ADCs:

- ADC1 (14-bit resolution) and ADC4 (12-bit resolution) for STM32U575/585, both up to 2.5 Msps
- ADC1 and ADC2 for STM32L5, with the same features

Compared to the STM32L5 ADC1 and ADC2, the STM32U575/585 ADC4 has the same resolution and does not support differential inputs and injected channels, but ADC4 supports the autonomous mode.

Table 76. ADC implementation in STM32L5 and STM32U575/585

Feature	STM32L5	STM32U575/585	
	ADC1 and ADC2	ADC1	ADC4
Resolution	12 bits	14 bits	12 bits
Maximum sampling speed	5 Msps	2.5 Msps	2.5 Msps
Hardware offset calibration	X		
Hardware linearity calibration	-	X	-
Single-ended inputs	X		
Differential inputs	X	X	-
Injected channel conversion	X	X	-
Oversampling	up to x256	up to x1024	up to x256
Data register	16 bits	32 bits	16 bits
DMA support	X		
Parallel data output to MDF	X (DFSDM)	X	-
Autonomous mode	-	-	X
Offset compensation	-	X	-
Gain compensation	-	X	-
Number of analog watchdogs	3		
Wakeup from Stop mode	-	-	X(1)

1. *Wakeup supported from Stop 0, Stop 1 and Stop 2 modes.*

The table below compares the STM32U575/585 ADC1 to the STM32L5 ADC1/2.

Table 77. ADC features in STM32L5 and STM32U575/585

Feature	STM32L5	STM32U575/585
	ADC1 and ADC2	ADC1
High-performance features	12-, 10-, 8- or 6-bit configurable resolution	14-, 12-, 10- or 8-bit configurable resolution
	ADC conversion time independent from the AHB bus clock frequency	
	Faster conversion time by lowering resolution	
	Manage single-ended or differential inputs	Management of single-ended or differential inputs (programmable per channels)
	AHB slave bus interface to allow fast data handling	
	Self-calibration	Self-calibration (both offset and linearity)

Feature	STM32L5	STM32U575/585
	ADC1 and ADC2	ADC1
High-performance features	Channel-wise programmable sampling time	
	N/A	Flexible sampling time control
	Up to four injected channels (fully configurable analog input assignment to regular or injected channels)	
	Hardware assistant to prepare the injected channel context and enable fast context switching	
	Data alignment with in-built data coherency	
	Data can be managed by DMA for regular channel conversions	Data management by general-purpose DMA for regular channel conversions with FIFO
	Data can be routed to DFSDM for post processing	Data routing to MDF for post processing
	Four dedicated data registers for the injected channels	
Dual ADC mode	Up to two ADCs that can operate in dual mode: • ADC1 is connected to 16 external channels + 3 internal channels. • ADC2 is connected to 16 external channels + 2 internal channels.	N/A
Oversampling	16-bit data register	32-bit data register
	Oversampling ratio adjustable from 2 to 256	Oversampling ratio adjustable from 2 to 1024
	Programmable data shift up to 8 bits	Programmable data right and left shift
Data preconditioning	N/A	Gain and offset compensation
Low-power features	• Speed adaptive low-power mode to reduce ADC consumption when operating at low frequency • Support of slow-bus frequency applications while keeping optimum ADC performance • Automatic control to avoid ADC overrun in AHB bus clock low-frequency application (auto-delayed mode)	
Channels and dedicated GPIOs pads	Up to 5 fast channels and 11 slow channels from GPIO pads	Up to 17 external analog input channels connected to dedicated GPIO pads
Internal channels	One channel for internal reference voltage (V_{REFINT}) and one channel for internal temperature sensor (V_{SENSE})	
	V_{BAT} monitoring channel ($V_{BAT}/3$), connected to ADC1	One channel for V_{BAT} monitoring ($V_{BAT}/4$)
	DAC1 and DAC2 internal channels connected to ADC2	DAC1 and DAC2 internal channels connected to ADC4
Start-of-conversion	Start-of-conversion can be initiated: • by software for both regular and injected conversions • by hardware triggers with configurable polarity (internal timers events or GPIO input events) for both regular and injected conversions	
Conversion modes	• Single mode: The ADC converts a single channel. The conversion is triggered by a special event. • Scan mode: The ADC scans and converts a sequence of channels. • Continuous mode: The ADC converts continuously selected inputs. • Discontinuous mode: The ADC converts a subset of the conversion sequence.	
Interrupt generation	An interrupt is generated when the ADC is ready: • at the end of sampling • at the end of the conversion (regular or injected) • by the analog watchdog 1, 2 or 3 • when an overrun event occurs	

Feature	STM32L5	STM32U575/585
	ADC1 and ADC2	ADC1
Analog watchdogs	The three watchdogs per ADC can perform filtering to ignore out-of-range data.	
ADC input range	ADC input range: $V_{REF-} \leq V_{IN} \leq V_{REF+}$	

9.2 Digital-to-analog converter (DAC)

STM32L5 and STM32U575/585 DAC peripheral have identical electrical parameters and configuration options, with only two differences in the new autonomous mode and double-data DMA capability for STM32U575/585:

- Autonomous mode to reduce the power consumption for the system

  The autonomous mode can be used to update the DAC output voltage in Stop mode. This allows DMA transfers to be performed when the device operates in Run, Sleep or Stop mode. The autonomous mode is supported only when the DAC is in sample-and-hold mode.
- Double-data DMA capability to reduce the bus activity

  When the DMA controller is used in normal mode, only 12-bit (or 8-bit) data are transferred by a DMA request. As the AHB width is 32 bits, two 12-bit data may be transferred simultaneously.

The DAC main features implemented in STM32U5 and STM32U575/585 are listed in the table below (refer to the product reference manual for more details).

Table 78. DAC features in STM32L5 and STM32U575/585

Feature	STM32L5	STM32U575/585
Dual channel	X	
Output buffer		
I/O connection	DAC1_OUT1 on PA4 and DAC1_OUT2 on PA5	
Maximum sampling time	1 Msps	
Autonomous mode	-	X
Double-data DMA		

9.3 Comparator (COMP)

The STM32L5 or STM32U575/585 devices embed two ultra-low-power comparators, COMP1 and COMP2, with the same electrical parameters and configuration options. These comparators can be used for a variety of functions including:

- Wakeup from low-power mode triggered by an analog signal
- Analog signal conditioning
- Cycle-by-cycle current control loop when combined with a PWM output from a timer

STM32U575/585 and STM32L5 AF pins of COMP instances are fully compatible and mapped as described in the table below.

Table 79. COMP AF pins in STM32L5 and STM32U575/585

AF pin function	STM32L5	STM32U575/585
COMP1_OUT	PB0, PB10	
COMP2_OUT	PB5, PB11	

9.4 Voltage reference buffer (VREFBUF)

The internal VREFBUF is an operational amplifier, with programmable gain. The amplifier input is connected to the internal voltage reference VREFINT.

STM32U575/585 and STM32L5 devices embed one VREFBUF that can be used as voltage reference for ADCs and DACs. VREFBUF can also be used as voltage reference for external components through the VREF+ pin.

The STM32U5 VREFBUF supports four voltages, when the STM32L5 one support only two voltages.

Table 80. VREFBUF features in STM32L5 and STM32U575/585

STM32L5		STM32U575/585	
Symbol	**Voltage (V)**	**Symbol**	**Voltage (V)**
-		VREFUBUF0	1.5
		VREFUBUF1	1.8
VREF_OUT1	2.048	VREFUBUF2	2.048
VREF_OUT2	2.5	VREFUBUF3	2.5

9.5 Operational amplifier (OPAMP)

The two OPAMP1 and OPAM2 (two inputs and one output each) in STM32U575/585 or STM32L5 devices have identical features. The three I/Os can be connected to the external pins to enable any type of external interconnections.

The OPAMP can be configured internally as a follower or as an amplifier with a non-inverting gain ranging from 2 to 16. The positive input can be connected to the internal DAC. The output can be connected to the internal ADC.

The only difference is that the STM32U575/585 OPAMP supports the high-speed mode and achieves a better slew rate.

10 Migration of signal/image processing accelerators

The STM32U575/585 devices embed a Chrom-ART Accelerator (DMA2D) that is a specialized DMA dedicated to image manipulation (not present in STM32L5).

The STM32U575/585 devices include also the following hardware accelerators and co-processors for signal processing:

- MDF (multi-function digital filter) and ADF (audio digital filter) that implement advanced architectures with new features versus the DFSDM (digital filter for sigma-delta modulators) implemented in STM32L5
- CORDIC co-processor and FMAC (filter mathematical accelerator) peripherals (not implemented in STM32L5)

10.1 MDF and ADF hardware digital filters

The STM32U575/585 devices implement two hardware digital filters, MDF and ADF. ADF features are a subset of the MDF ones. However, the ADF includes a dedicated module to sound activity detection with wakeup. MDF and ADF are, like the DFSDM in STM32L5, high-performance dedicated modules intended to interface external ΣΔ modulators. MDF and ADF also feature parallel data stream input from internal ADC peripherals.

MDF and ADF can connect external sensors and DFSDM can acquire parallel data stream input from internal device memory. MDF and ADF are functional in Stop 0 and Stop 1 modes according to autonomous mode feature. In addition, the ADF is autonomous in Stop 2 mode: mapped to the AHB3 bus in SRD, the ADF is capable to wake up from Stop 2 mode.

Table 81. Digital filter features in STM32L5 and STM32U575/585

Feature	STM32L5	STM32U575/585	
	DFSDM1	ADF1	MDF1
Number of filters and interfaces	4 internal 16-bits data channels	1 DFLT (digital filter) and 1 SITF (serial interface)	6 DFLT and 6 SITF
MDF_CKIy/MDF_CKI0 connected to pins	N/A	-	X
ADF_CKI0 connected to pins	N/A	X	-
Sound activity detection (SAD)	N/A	X	-
RxFIFO depth (number of 24-bit words)	N/A[1]	4	
Number of RxFIFO		1	4
Motor dedicated features: SCD (short-circuit detector), OLD (out-of-limit detector), OEC (offset error cancellation), INT (integrators), snapshot, break	X	-	X (with advanced features)
Main path with CIC4, CIC5	X		
Main path with CIC1/2/3 or FastSinc	X	-	X
RSFLT (reshape filter), HPF (high-pass filter), SAT (saturation blocks), SCALE, DLY, Discard functions	-[2]	X	
Autonomous in Stop modes	-	X (Stop 0, Stop 1 and Stop 2)	X (Stop 0 and Stop 1)
Input from internal ADC	X	-	X (ADC1 connected to ADCITF1 and ADCITF2)

Feature	STM32L5	STM32U575/585	
	DFSDM1	ADF1	MDF1
Supported trigger sources	32	1	14
Flexible matrix (BSMX) for connection between filters and digital inputs	-	X	

1. *The maximum output data resolution is up to 24 bits. DFSDM does n0t include a FIFO. The data can be automatically stored in a system RAM buffer through DMA.*
2. *Only pulses skipper equivalent to clock skipper delay in STM32U575/585 (DLY).*

STM32U575/585 and STM32L5 AF pins of MDF/DFSDM are mapped as described in the table below.

Table 82. MDF/DFSDM AF pins in STM32L5 and STM32U575/585

AF pin function	DFSDM1 in STM32L5	MDF1 in STM32U575/585
MDF1_CCK0	N/A	PB8, PE9, PG7
MDF1_CCK1		PC2, PF10
MDF1_CKIN0	PB2, PD4	
MDF1_CKIN1	PB13, PD7	
MDF1_CKIN2	PB15, PE8	
MDF1_CKIN3	PC6, PE5	
MDF1_CKIN4	N/A	PC1, PE11
MDF1_CKIN5		PB7, PE13
MDF1_SDIN0	PB1, PD3	
MDF1_SDIN1	PB12, PD6	
MDF1_SDIN2	PB14, PE7	
MDF1_SDIN3	PC7, PE4	
MDF1_SDIN4	N/A	PC0, PE10
MDF1_SDIN5		PB6, PE12
DFSDM1_CKOUT	PB8, PC2, PE9, PF10, PG7	N/A

STM32U575/585 AF pins of ADF are mapped as described in the table below (no ADF on STM32L5 Series).

Table 83. ADF AF pins in STM32U575/585

AF pin function	STM32U575/585
ADF1_CCK0	PB3, PE9
ADF1_CCK1	PC10
ADF1_SDIN0	PB4, PC11, PE10

10.2 CORDIC

The CORDIC co-processor provides hardware acceleration of certain mathematical functions (mainly trigonometric ones) commonly used in motor control, metering, signal processing and many other applications.

The CORDIC speeds up the calculation of these functions compared to a software implementation, making it possible the use of a lower operating frequency, or freeing up processor cycles in order to perform other tasks.

The cording main features are the following:

- 24-bit CORDIC rotation engine
- Circular and Hyperbolic modes
- Rotation and Vectoring modes
- Functions: sine, cosine, sinh, cosh, atan, atan2, atanh, modulus, square root, natural logarithm
- Programmable precision
- Low-latency AHB slave interface
- Results readable as soon as ready, without polling or interrupt
- DMA read and write channels
- Multiple register read/write by DMA

10.3 FMAC

The FMAC is implemented on STM32U575/585 only. The FMAC performs arithmetic operations on vectors. It comprises a multiplier/accumulator (MAC) unit, together with address generation logic that allows FMAC to index vector elements held in local memory.

The FMAC main features are the following:

- 16 x 16-bit multiplier
- 24 + 2-bit accumulator with addition and subtraction
- 16-bit input and output data
- 256 x 16-bit local memory
- Up to 3 areas in memory for data buffers (two inputs, one output) can be defined by programmable base address pointers and associated size registers
- Circular input and output buffers
- Filter functions: FIR, IIR (direct form 1)
- Vector functions: dot product, convolution, correlation
- AHB slave interface
- DMA read and write data channels

10.4 Touch sensing controller (TSC)

The STM32U575/585 and STM32L5 embed a touch sensing controller (TSC) with same features. The TSC provides a simple solution to add capacitive-sensing functionality to any application. A capacitive-sensing technology can detect a finger presence near an electrode that is protected from direct touch by a dielectric (such as glass or plastic). The capacitive variation introduced by the finger (or any conductive object) is measured using a proven implementation based on a surface charge transfer acquisition principle. Refer to the STM32U585/575 reference manual (RM0456) for more details of TSC features).

The number of capacitive-sensing channels is dependent on the size of the package and subject to I/O availability. The TSC input/output signals and their pins mapping are fully compatible between STM32L5 and STM32U575/585.

STM32U575/585 Series AF pins of TSC are fully compatible and mapped as described in the table below.

Table 84. TSC AF pins in STM32L5 and STM32U575/585

AF pin function	STM32L5	STM32U575/585
TSC_SYNC	PB10, PD2	
TSC_G1_IO1	PB12	
TSC_G1_IO2	PB13	
TSC_G1_IO3	PB14	
TSC_G1_IO4	PC3	
TSC_G2_IO1	PB4	

AF pin function	STM32L5	STM32U575/585
TSC_G2_IO2	PB5	
TSC_G2_IO3	PB6	
TSC_G2_IO4	PB7	
TSC_G3_IO1	PC2	
TSC_G3_IO2	PC10	
TSC_G3_IO3	PC11	
TSC_G3_IO4	PC12	
TSC_G4_IO1	PC6	
TSC_G4_IO2	PC7	
TSC_G4_IO3	PC8	
TSC_G4_IO4	PC9	
TSC_G5_IO1	PE10	
TSC_G5_IO2	PE11	
TSC_G5_IO3	PE12	
TSC_G5_IO4	PE13	
TSC_G6_IO1	PD10	
TSC_G6_IO2	PD11	
TSC_G6_IO3	PD12	
TSC_G6_IO4	PD13	
TSC_G7_IO1	PE2	
TSC_G7_IO2	PE3	
TSC_G7_IO3	PE4	
TSC_G7_IO4	PE5	
TSC_G8_IO1	PF14	
TSC_G8_IO2	PF15	
TSC_G8_IO3	PG0	
TSC_G8_IO4	PG1	

11 Migration of external-memory interface peripherals

The STM32U575/585 devices implement two peripherals dedicated to external-serial memories: OCTOSPI and FSMC. The STM32U5 FSMC shares the same features with the STM32L5 one. The STM32U575/585 embed the same OCTOSPI features than the STM32L5, with updates related to the I/O management.

11.1 Octo-SPI interface

The OCTOSPI peripheral provides a serial interface that enables communication with external serial memories such as Flash memory, PSRAM, HyperRAM™, HyperFlash™ and some specific circuits like FPGA or ASICs.

The Octo-SPI specialized communication interface targets single-, dual-, quad- or octal-SPI memories. The OCTOSPI can be configured in three modes: Indirect mode, Status-polling mode and Memory-mapped mode.

The OCTOSPI I/O manager (OCTOSPIM) is a hardware peripheral that implements a low-level interface that enables:

- an efficient OCTOSPI pin assignment with a full I/O matrix (before alternate function map)
- multiplex of single-, dual-, quad- or octal-SPI interfaces over the same bus

Table 85. OCTOSPI features in STM32L5 and STM32U575/585

Feature	STM32L5	STM32U575/585
Number of instances	OCTOSPI1	OCTOSPI1 and OCTOSPI2
OCTOSPI I/O manager (OCTOSPIM)	N/A	X
Other features	Same features	

STM32U575/585 and STM32L5 Series AF pins of OCTOSPI/OCTOSPIM instances are fully compatible and mapped as described in the table below (no OCTOSPIM2 in STM32L5).

Table 86. OCTOSPIM AF pins in STM32L5 and STM32U575/585

AF pin function	STM32L5	STM32U575/585
OCTOSPIM_P1_CLK	PA3, PB10, PE10, PF10	
OCTOSPIM_P1_NCLK	PB5, PB12, PE9, PF11	
OCTOSPIM_P1_DQS	PA1, PB2, PE3, PG6	
OCTOSPIM_P1_NCS	PA2, PA4, PB11, PC11, PE11	
OCTOSPIM_P1_IO0	PB1, PE12, PF8	
OCTOSPIM_P1_IO1	PB0, PE13, PF9	
OCTOSPIM_P1_IO2	PA7, PE14, PF7	
OCTOSPIM_P1_IO3	PA6, PE15, PF6	
OCTOSPIM_P1_IO4	PA6, PE15, PF6	
	N/A	PH2
OCTOSPIM_P1_IO5	PC2, PD5, PG11	
	N/A	PI0
OCTOSPIM_P1_IO6	PC3, PD6	
OCTOSPIM_P1_IO7	PC0, PC4, PD7	
OCTOSPIM_P2_CLK	N/A	PF4, PH6, PI6
OCTOSPIM_P2_NCLK		PF5, PH7, PI7
OCTOSPIM_P2_DQS		PF12, PG7, PG15, PH4

AF pin function	STM32L5	STM32U575/585
OCTOSPIM_P2_NCS	N/A	PD3, PG12, PI5, PI8
OCTOSPIM_P2_IO0		PF0, PI3
OCTOSPIM_P2_IO1		PF1, PI2
OCTOSPIM_P2_IO2		PF2, PI1
OCTOSPIM_P2_IO3		PF3, PH8
OCTOSPIM_P2_IO4		PG0, PH9
OCTOSPIM_P2_IO5		PG1, PH10
OCTOSPIM_P2_IO6		PG9, PH11, PH15
OCTOSPIM_P2_IO7		PG10, PH12

11.2 Flexible static memory controller (FSMC)

The STM32U575/585 FSMC peripheral shares the same features as the STM32L5 one. It includes two memory controllers:

- NOR/PSRAM memory controller
- NAND memory controller

The FSMC can interface with synchronous and asynchronous static memories, and NAND Flash memory. FSMC main purposes are:

- to translate AHB transactions into the appropriate external device protocol
- to meet the access time requirements of the external memory devices

Table 87. FSMC features in STM32L5 and STM32U575/585

Feature	STM32L5	STM32U575/585
External memory interfaces supported	• external SRAM • NOR Flash memory/OneNAND Flash memory • PSRAM (4 memory banks) • Ferroelectric RAM (FRAM) • NAND Flash memory with ECC hardware to check up to 8 Kbytes of data	
Interface with parallel LCD modules, supporting Intel® 8080 and Motorola 6800 modes	X	
Burst mode support for faster access to synchronous devices (such as NOR Flash memory or PSRAM)		
Programmable continuous clock output for asynchronous and synchronous accesses	8-,16-bit wide data bus	
Independent chip select control for each memory bank	X	
Independent configuration for each memory bank		
Write enable and byte lane select outputs for use with PSRAM, SRAM devices		
External asynchronous wait control		
Write FIFO depth	16 x32-bit depth	

STM32U575/585 and STM32L5 AF pins of FSMC are fully compatible. They are mapped as described in the table below.

Table 88. FSMC AF pins in STM32L5 and STM32U575/585

AF pin function	STM32L5	STM32U575/585
FMC_CLK	PD3	
FMC_NL	PB7	
FMC_NBL0	PE0	
FMC_NBL1	PE1	
FMC_NOE	PD4	
FMC_NWE	PD5	
FMC_NWAIT	PD6	
FMC_NCE/FMC_NE1	PD7	
FMC_NCE/FMC_NE2	PG9	
FMC_A0	PF0	
FMC_A1	PF1	
FMC_A2	PF2	
FMC_A3	PF3	
FMC_A4	PF4	
FMC_A5	PF5	
FMC_A6	PF12	
FMC_A7	PF13	
FMC_A8	PF14	
FMC_A9	PF15	
FMC_A10	PG0	
FMC_A11	PG1	
FMC_A12	PG2	
FMC_A13	PG3	
FMC_A14	PG4	
FMC_A15	PG5	
FMC_A16	PD11	
FMC_A17	PD12	
FMC_A18	PD13	
FMC_A19	PE3	
FMC_A20	PE4	
FMC_A21	PE5	
FMC_A22	PE6	
FMC_A23	PE2	
FMC_A24	PG13	
FMC_A25	PG14	
FMC_D0	PD14	
FMC_D1	PD15	

AF pin function	STM32L5	STM32U575/585
FMC_D2	PD0	
FMC_D3	PD1	
FMC_D4	PE7	
FMC_D5	PE8	
FMC_D6	PE9	
FMC_D7	PE10	
FMC_D8	PE11	
FMC_D9	PE12	
FMC_D10	PE13	
FMC_D11	PE14	
FMC_D12	PE15	
FMC_D13	PD8	
FMC_D14	PD9	
FMC_D15	PD10	

12 Software migration

12.1 Reference documents

Check the following documents for more details:

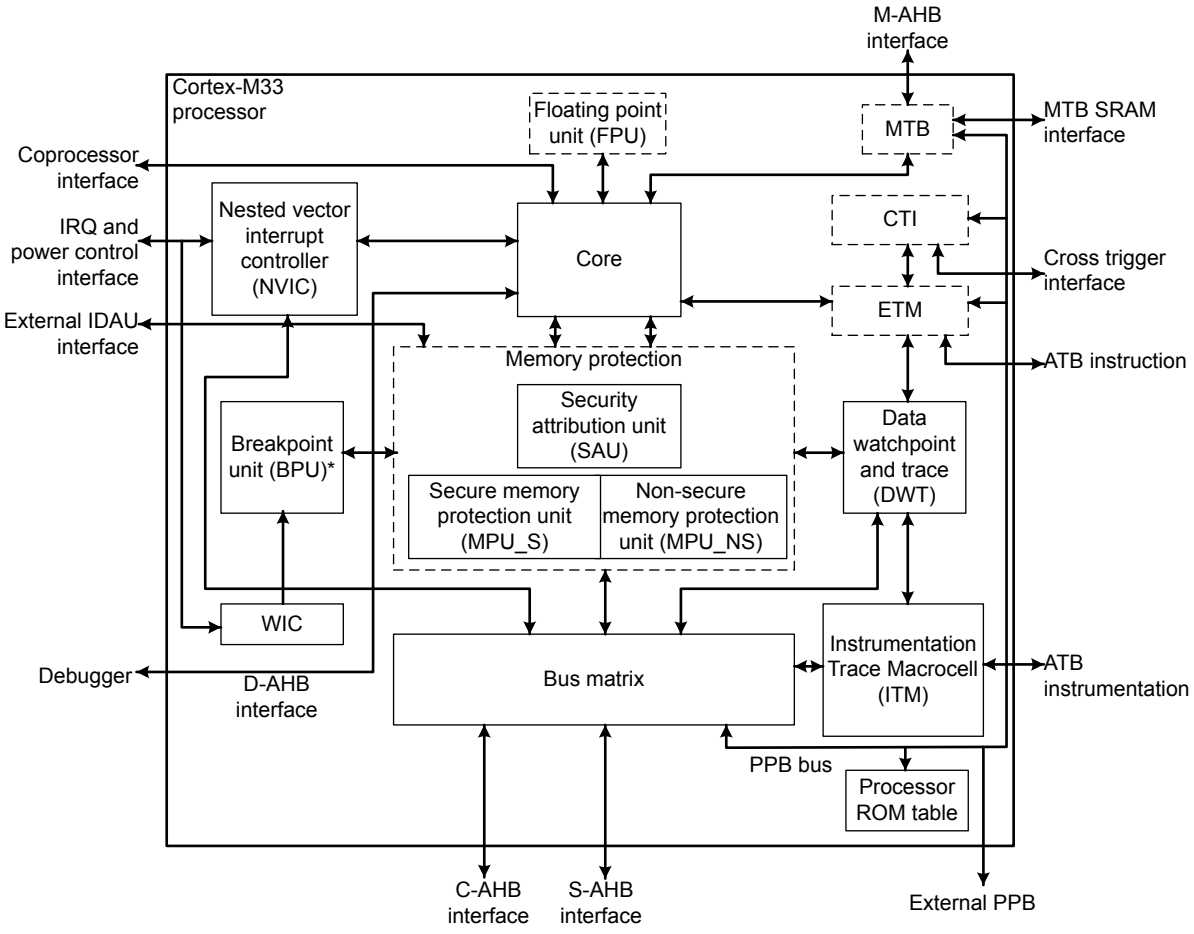
- Definitive guide for Arm Cortex-M33 and Cortex-M4 processors
- Cortex-M33 Processor Technical Reference Manual, available on Arm website

12.2 Cortex-M33 overview

The Cortex-M33 processor is excellence in ultra-low-power, performance and security. This processor is based on the Armv8-M architecture for use in environments requiring more security implementation. The Cortex-M33 core implements a full set of DSP (digital signal processing) instructions, TrustZone aware support and a memory protection unit (MPU) that enhances the application security.

The Cortex-M33 core also features a single-precision floating-point unit (FPU), that supports all the Arm single-precision data-processing instructions and all the data types. The STM32 Cortex-M33 implementation is illustrated in the figure below.

Figure 3. STM32 Cortex-M33 implementation



* Flash patching is not supported in the Cortex-M33 processor.

Cortex-M33 key features are listed below:

- Arm-v8M architecture with 2/3 stage pipeline, Harvard, 1,4 DMIPS/MHz
- Single-cycle branch, no branch prediction
- Hardware divide instruction
- Debug (CoreSight compliant)
- Memory exclusive instructions
- NVIC without interrupts increased up to 480 max (256 priority levels)
- Enhanced MPU, more flexible (32 bytes) up to 16 regions (for each one of the secure and non-secure states)
- New AMBA® 5 AHB interface, support of security state extension to the system
- Support of external implementation defined attribution unit
- Fully compatible with TrustZone system

12.3 Cortex-M33 software point of view

The Cortex-M33 includes the following features:

- Implementing Armv8-M architecture
- Implementing the latest FPU specification (based on Arm FPv5 architecture)
- Using the AHB5 specification for the system and memory interface to extend security across the whole system
- Using the latest version of the MPU specification to simply the setup of regions
- Extends the number of maximum interrupts to 480
- Optional execution trace using MTB or ETM
- Enhanced debug components to make simplify usage
- Coprocessor interface supporting up to eight coprocessors units
- Hardware stack limit checking
- TrustZone security features adding efficient security features

12.4 Cortex-M33 mapping overview

The mapping on cortex-M33 is illustrated on the table below.

Table 89. Cortex-M33 overview mapping for STM32L5 and STM32U575/585

STM32L5 and STM32U575/585		
Architecture		**Cortex-M33**
Core	NVIC (nested vectored interrupt controller)	109 maskable interrupt channels (not including the 16 interrupt lines of the Cortex-M33 with FPU)
	EXTI (extended interrupts and events controller)	43 event/interrupt
Mapping	System timer	0xE000 E010 to 0xE000 E0FF
	NVIC	0xE000 E100 to 0xE000 ECFF
	MPU	0xE000 ED90 to 0xE000 EDB8
	FPU	0xE000 EF30 to 0xE000 EF44

13 Conclusion

This application note is a complement to the STM32L5 and STM32U575/585 datasheets and reference manuals. This document provides a simple guideline to migrate an existing product based on STM32L5 to the STM32U575/585 devices.

Revision history

Table 90. **Document revision history**

Date	Version	Changes
21-May-2021	1	Initial release.

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