AN2156
APPLICATION NOTE

STR73x Family
STR73x Hardware Getting Started

Introduction

The aim of this application note is to give users of the STR73x family devices a number of recommendations on the HW circuitry connected to the main special pins. It covers the pins for power supply (digital and analog), reset, crystal oscillator, the decoupling of the internal voltage regulator, boot modes, test pin, RC oscillator biasing pin and the JTAG debug port.

Detailed reference design schematics of the STR730-EVAL board are also contained in this document with descriptions of the main components, interfaces and modes.

Contents

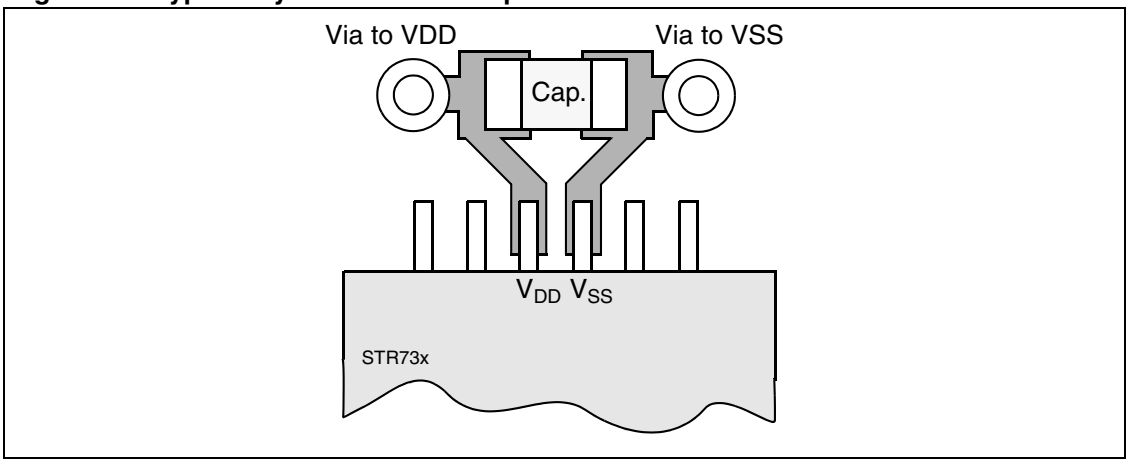
1 Power management

1.1 Power supply pins VDD/VSS

All current STR73x devices are supplied with a nominal voltage of 5V. The power supply pins are organized in VDD/VSS pairs around the chip and exceptionally all pins need to be properly connected to the power supplies, VDD to 5V, VSS to GND. These connections including pads, tracks and vias should have an impedance as low as possible. This is typically achieved with thick track widths and preferably dedicated power supply planes in multi layer PCBs.

In addition, each VDD/VSS pair should be decoupled with ceramic capacitors which need to be placed as close as possible to the appropriate pins or below the pins on the contrary side of the PCB. Typical values are 10nF to 100nF, but exact values depend on the application needs. The following figure shows the typical layout on such a VDD/VSS pair.

Figure 1. Typical layout for VDD/VSS pair



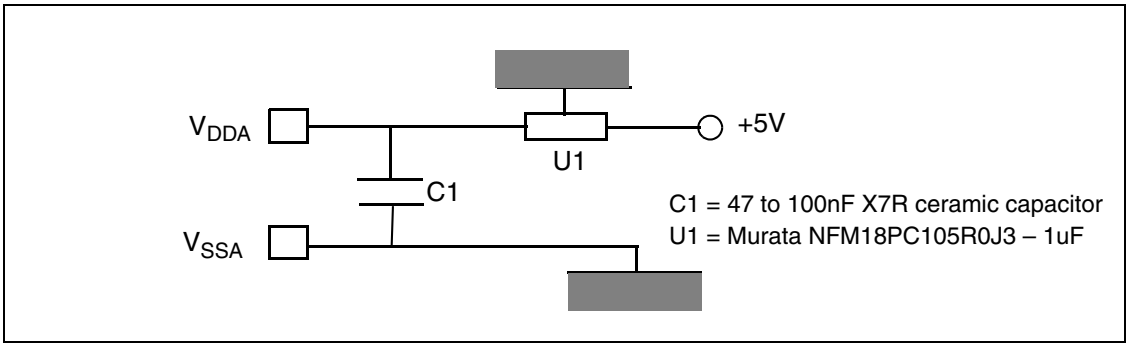
1.2 Analog supply and reference V_{DDA}/V_{SSA}

The V_{DDA} pin is used to supply the ADC and to provide it with the analog reference.

As for the supply pins, V_{DDA}/V_{SSA} decoupling with short connections is recommended and an X7R ceramic capacitor of 47nF to 100nF can be used for this.

When full accuracy is needed, and depending on the noise rejection of the voltage regulator used to supply the STR73x device, a low pass filter may be considered. As the pin is also used as the ADC supply, the use of a serial resistor must be avoided to reduce the risk of offset error generation. An EMI component from Murata is proposed instead.

Figure 2. V_{DDA}/V_{SSA} decoupling with an X7R ceramic capacitor



1.3 Decoupling of the internal voltage regulator V18

All existing STR73x derivates are supplied with a single external voltage of 5V. The additional voltages needed are generated by internal charge pump circuits for the flash programming/ erasing and an internal linear voltage regulator which provides the 1.8V for the internal logic. The output of the internal voltage regulator is connected to one or two pins V18, where an external capacitance needs to be connected for decoupling/stabilization between the V18 pin and VSS/GND. There are two important notes:

1. V18 is probably the most critical pin regarding EMC emissions. Therefore the external capacitor(s) must be placed as close as possible (few mm) to the V18/VSS pair(s) or below on the other side of the PCB. If this is done, a very good EMC performance can be achieved.
2. Depending on the device, different capacitances are needed. The values mainly depend on the type of the internal voltage regulator used. Please refer to the tables below which cover the devices available or planned at the time of writing. In case of future devices which are not covered by this application note please refer to the datasheet or contact your support engineer.

The figure below shows the two affected pins (V18 and VBias) of the TQFP144 package as well as the TQFP100 package. In order to support all devices with a single PCB design, it is necessary to provide on both pins footprints for 10µF tantalum and 47-100nF ceramic capacitors. The footprint for the ceramic capacitor on pin 64 should be reusable to be soldered with a resistor instead for the biasing functionality. This may be achieved with 0805 or 0603 SMD footprints. Please refer to the tables below for the different component values and assembly options depending upon the device derivate.

Figure 3. Pin availability for V18 functionality

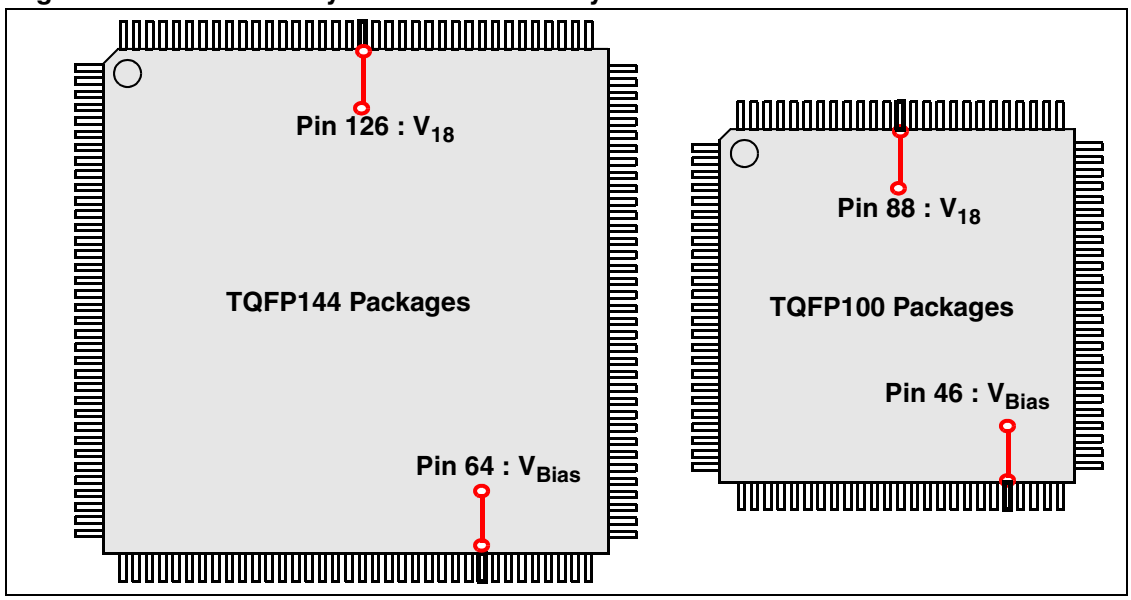


Table 1. Component values for TQFP144 package

Package	Derivate	CMU / RC osc.	Pin 64			Pin 126		
			Function	Component	Value	Function	Component	value
TQFP144/ LFBGA144	STR730 STR735	yes	VBias	resistor (*)	1.3MΩ	V18	ceramic cap	100nF

(*) only necessary for 32kHz mode of RC oscillator

Table 2. Component values for TQFP100 package

Package	Derivate	CMU / RC osc.	Pin 46			Pin 88		
			Function	Component	Value	Function	Component	value
TQFP100	STR731 STR736	yes	VBias	resistor (*)	1.3MΩ	V18	ceramic cap	100nF

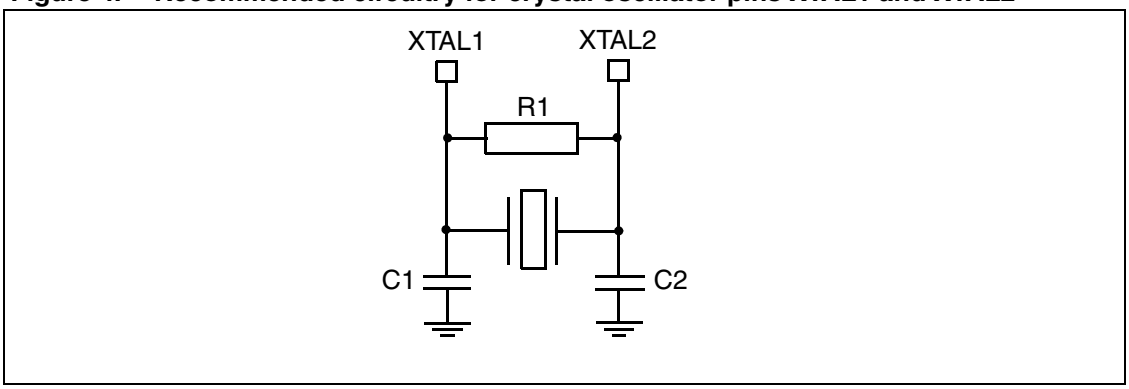
(*) only necessary for 32kHz mode of RC oscillator

2 Clock management

2.1 Crystal oscillator pins XTAL1, XTAL2

All current STR73x devices have an on-chip oscillator that allows the driving of external crystals or resonators with a fundamental frequency of 4-8 MHz. The recommended circuitry for a crystal is shown below. C1, C2 and R1 values depend greatly on the crystal type and manufacturer. It is suggested that you ask your crystal supplier for the best values for these components.

Figure 4. Recommended circuitry for crystal oscillator pins XTAL1 and XTAL2



Resistor R1 is recommended for feedback stability and has a value of around 1MΩ. As the oscillator of STR73x devices has automatic gain control, there is no need to add a resistance in series.

The values of the load capacitors C1 and C2 are also heavily dependent on the crystal type and frequency. For best oscillation stability they normally have the same value. Typical values are in the range from below 10pF up to 30pF. The parasitic capacitance of the board layout also needs to be considered and typically adds a few pF to the component values.

In the PCB layout all connections should be as short as possible. Any additional signals, especially those that could interfere with the oscillator, should be locally separated from the PCB area around the oscillation circuit using suitable shielding.

2.2 On-chip RC oscillator and VBias pin

All devices of the STR73x family have an on-chip RC oscillator in addition to the main oscillator. This on-chip RC oscillator is capable of running at either 2MHz or 32kHz.

- The default 2MHz mode requires no external components.
- The 32 kHz mode requires an external bias resistor of 1.3 MΩ from the VBias pin towards GND.

Note: The oscillator frequencies can be adjusted through software after reset, where the reset frequencies are around 2.34Mhz / 29Khz.

3 Reset management

3.1 Reset pin nReset

All current STR73x devices are specified for a nominal voltage of 5V with a tolerance of ±10%, thus between 4.5V and 5.5V. The external reset circuitry should apply a reset whenever the supply voltage is outside this voltage supply range and only release it when inside the supply range.

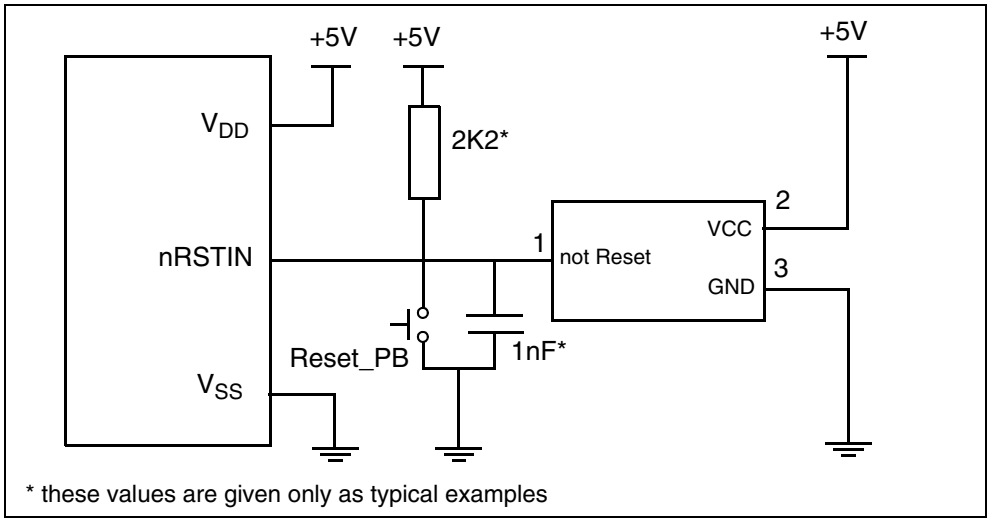
Being within the supply range of 5V ±10%, the absolute minimum duration of the hardware reset pulse is 100µs, but it is recommended that the reset circuitry adds increased time margin, e.g. 200µs.

Note: During power-on, a reset must be provided externally.

At power-on, the nRSTIN pin must be held low by an external reset circuit until V_{DD} is reached. *Figure 5* gives an example of the hardware implementation of the RESET circuit for STR73x devices.

The STM1001 low-power CMOS microprocessor supervisory circuit is used to assert a reset signal whenever the V_{DD} voltage falls below a preset threshold or whenever a manual reset is asserted.

Figure 5. Hardware reset implementation



4 Boot management

4.1 SystemMemory / User Boot mode pins M0, M1

The recommended circuitry around the mode pins M0 and M1 depends upon the end of line programming strategy for virgin devices. The device always operates (i.e. executes the application) in user boot mode and it is also possible to program the device via the JTAG debug port in this mode. Field updates, where the application is already running and updating itself, also use this mode. Depending solely on the application, any interface may be used for field updates such as CAN or UART.

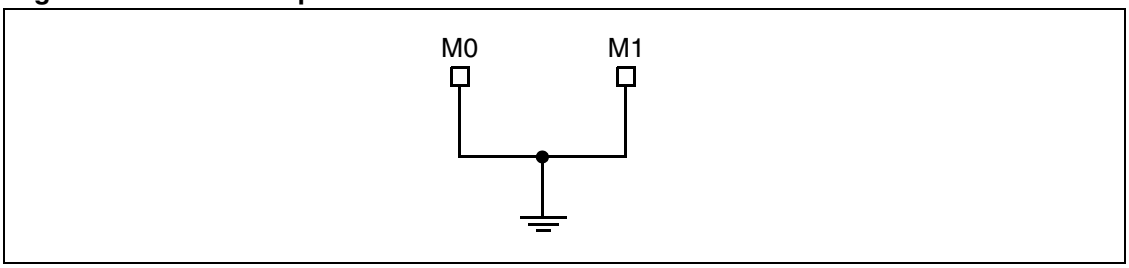
The support of SystemMemory boot mode is necessary only when virgin devices or applications which are not able to update themselves, are programmed via CAN or UART. Please note that circuitry is needed that supports both user and SystemMemory boot modes.

ST prefers programming via the JTAG port, since it provides the fastest possible method, no interface resources are necessary, the handling is easier and a lot of professional end-of-line programming solutions already exist from well known companies such as PLS and BP Microsystems.

4.1.1 End of line programming via JTAG

If you know already that you will program the devices only via the JTAG debug port, simply connect both mode pins M0 and M1 directly or via pull-down resistors to GND.

Figure 6. M0 and M1 pin connections



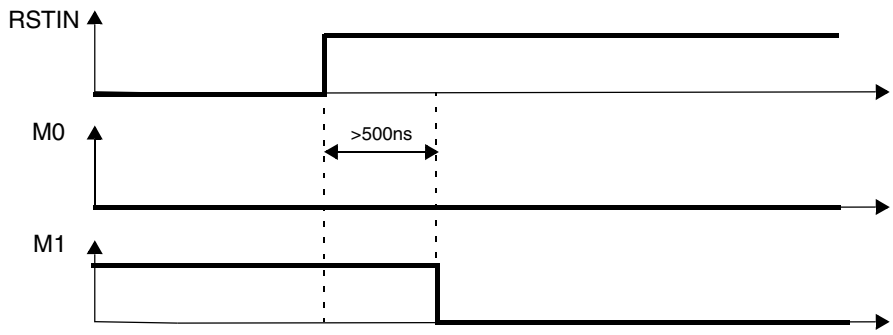
4.1.2 End of line programming via UART or CAN

If you are not yet sure which end of line programming method to use or you know that you will use the SystemMemory boot mode method, you need dynamic handling of the mode pins.

The voltage levels on the mode pins are latched with a rising edge on the reset pin. When both M0 and M1 are low at this time then user boot mode is entered. When M0 is low and M1 high at this time then SystemMemory boot mode is entered and the testflash sector is aliased at address 0 instead of the normal sector 0.

As long as M1 stays high the clock is stretched and no code is executed. So in order to run the bootstraploader code of the testflash sector a falling edge on M1 is needed some time after the rising edge on reset. This time is not critical but must exceed 500ns. The following figure shows the timing.

Figure 7. Timing diagram for RSTIN, M0 and M1

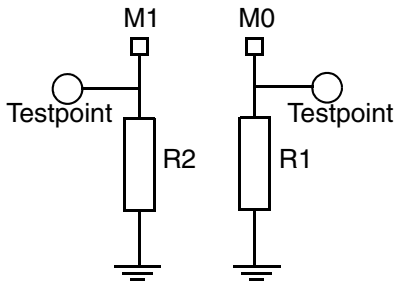


Latching of M0 and M1

SystemMemory Boot mode with support of external HW such as a Tester

The easiest way to support the SystemMemory boot mode without adding much complexity and cost is to replace the direct connection of M0 and M1 pins towards GND with pull-down resistors and to add one test pin each directly connected to M0 and M1. The pull-down resistors should have a value of around 10kΩ. If no further hardware is connected to the testpins the user boot mode will be selected. If however a tester provides the necessary dynamic voltages to the testpins via a needle adaptor the SystemMemory bootmode can be used.

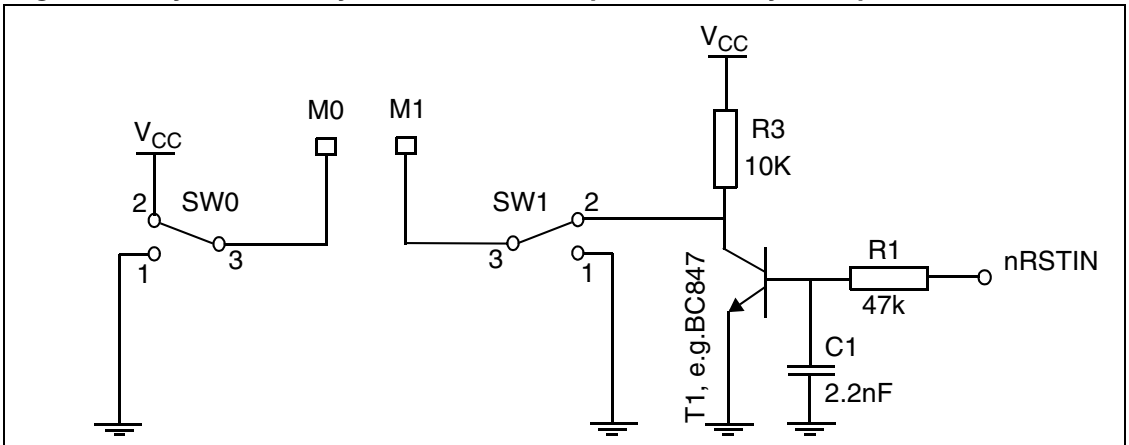
Figure 8. M1 and M0 connections giving support for external tester



SystemMemory Boot mode with onboard circuitry

The necessary dynamic signals can also be generated by onboard circuitry so that no external hardware is necessary. The following schematic shows how this could be done. During active reset (nRSTIN low) the transistor is in high impedance and the capacitor is uncharged through the two resistors R1, resulting in M1 being high. As soon as the reset signal is deasserted high the transistor switches to low impedance after the charge of the capacitor via resistor R1 and R3.(when the Vbe of the transistor is upper than 0.7V). As a consequence M0 will become low after a period of a few µs.

Figure 9. SystemMemory Boot mode development circuitry example

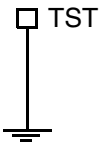


SW0: 1-3 & SW1:1-3 User Boot Mode 1
SW0: 2-3 & SW1:1-3 User Boot Mode 2
SW0: 1-3 & SW1:2-3 SystemMemory Boot Mode
SW0: 2-3 & SW1:2-3 Reserved

4.2 Test mode

The TST pin must always be connected to GND to disable testmode. Testmode is ST's reserved mode and must never be used by the application.

Figure 10. TST pin connection



5 Debug management

5.1 JTAG debug port pins

The JTAG interface is a special synchronous serial port and provides access to the internal scanchains and the debug logic. Some of these scanchains are around the ARM core and the Embedded ICE Unit. With these it is possible to insert data into and read from the processor's pipeline, to program breakpoints and watchpoints and to control the debugging.

Since the JTAG port is an integral part of the ARM core it is available on every device and thus also allows in-system debugging and in-system flash-programming directly in the target application. The JTAG interface pins consist of the following signals:

Table 3. JTAG interface signals

Std name	STR73x name	Direction/Description	Function
nTRST	JTRST	Test Reset (from JTAG equipment)	This active LOW open-collector is used to reset the JTAG port and the associated debug circuitry. It is asserted at power-up by each module, and can be driven by the JTAG equipment.
TDI	JTDI	Test data in (from JTAG equipment)	TDI goes down the stack of modules to the motherboard and then back up the stack, labelled TDO, connecting to each component in the scan chain.
TMS	JTMS	Test mode select (from JTAG equipment)	TMS controls transitions in the tap controller state machine. TMS connects to all JTAG components in the scan chain as the signal flows down the module stack.
TCK	JTCK	Test clock (from JTAG equipment)	TCK synchronizes all JTAG transactions. TCK connects to all JTAG components in the scan chain. Series termination resistors are used to reduce reflections and maintain good signal integrity. TCK flows down the stack of modules and connects to each JTAG component. However, if there is a device in the scan chain that synchronizes TCK to some other clock, then all down-stream devices are connected to the RTCK signal on that component.
RTCK	GND (not used)	Return TCK (to JTAG equipment)	Some devices sample TCK (for example a synthesizable core with only one clock), and this has the effect of delaying the time that a component actually captures data. Using a mechanism called adaptive clocking, the RTCK signal is returned by the core to the JTAG equipment, and the clock is not advanced until the core had captured the data. In adaptive clocking mode, the debugging equipment waits for an edge on RTCK before changing TCK.

Std name	STR73x name	Direction/Description	Function
TDO	JTDO	Test data out (to JTAG equipment)	TDO is the return path of the data input signal TDI.
nSRST	nRSTIN	System reset (bidirectional)	nSRST is an active LOW open-collector signal that can be driven by the JTAG equipment to reset the target board. Some JTAG equipment senses this line to determine when a board has been reset by the user. When the signal is driven LOW by the reset controller on the core module, the motherboard resets the whole system by driving nSYSRST low.
DBGRQ	GND (not used)	Debug request (from JTAG equipment)	DBGRQ is a request for the processor core to enter debug state.
DBGACK	GND (not used)	Debug acknowledge (to JTAG equipment)	DBGACK indicates to the debugger that the processor core has entered debug mode.

The JTAG input signals have weak internal pull-up and pull-down resistors, but these are not always active:

- When debug protection is activated (JTAG permanently held in reset internally)
- At power up and down there may be a short duration where the power on reset is already released internally, but where the resistors are not yet active.

To avoid any floating input pins even for a very short period it is highly recommended to always provide additional external pull-up and pull-down resistors. This recommendation is valid whether the JTAG port is used or not.

The following table shows the recommended values and types:

Table 4. Recommended JTAG debug port components

Signal name	Recommended external Resistor type	Recommended value
JTCK	Pull-down between pin and VSS/ GND	10kΩ
JTDI	Pull-up between pin and VDD/ VCC	10kΩ
JTDO	Output, no resistor needed	N.A.
JTMS	Pull-up between pin and VDD/ VCC	10kΩ
JTRST	Pull-down (*) between pin and VSS/GND	10kΩ

To connect the target with a debugger some additional signals are needed, mainly the System Reset nRSTIN, so that the debugger can also reset the whole MCU, not only the JTAG part. nRSTIN should be an open collector so that the different reset sources (power-on reset circuitry, ext. watchdog if available and the JTAG equipment/Debugger) can be connected together. The Debugger itself will also monitor the level on nRSTIN, so that it recognizes when a reset is forced by some other circuitry.

Finally the target supply voltage must be provided so that the Debugger may adapt voltage levels appropriately.

All signals should be made accessible at least as testpoints that can then be fed via some needle adaptors to the ARM standard JTAG connector. If cost and space allow, the connector can also be directly put on the target PCB. The connector is a standard two row, 20-pin header connector with a pitch of 0.1 inch / 2.54 mm and should have a collar to avoid incorrect mounting.

6 Reference design

6.1 Main

The STR730-EVAL board is based on the STR730FZ2T7, a highly integrated microcontroller, running at up to 36 MHz that uses the popular ARM7TDMI™ 32-bit RISC CPU featuring on-chip high speed single voltage flash memory and high-speed RAM, clock generation via PLL, and numerous on-chip peripherals.

6.2 Clock

Clocking is performed by a +5 V surface mounted 8 MHz quartz. Please refer to the *Section 2.1: Crystal oscillator pins XTAL1, XTAL2* for more details.

6.3 Reset

One push button SW_PB:S100 is used to generate a hardware reset. Please refer to the *Section 3: Reset management* for more details.

6.4 Boot mode

The are three different modes available and can be enabled by means of two dedicated Input only pins:

User Boot Mode 1: In this mode, Flash sector B0F0 is mapped in both Block 010 and Block 000 of the memory map. The system boots from block 0, segment 0 of Flash (normal operation)

User Boot Mode 2: This mode has the same mapping as User Boot mode 1 except Flash sector B0F1 is reserved and any attempt to access address range 0x8000 2000 to 0x8000 3FFF will generate an ABORT.

SystemMemory Boot mode: This mode has the same mapping as User Flash boot mode 1, except that the SystemMemory flash sector is accessible in address range 0x8010 C000 to 0x8010 DFFF and is aliased in Block 0 This allows the system to boot from SystemMemory (for initial Flash Programming).

Please refer to the *Section 4: Boot management* for more details.

6.5 Wake-Up

Push button S103 is connected to Wake-up line 16 and is used to exit from Stop mode.

For more details, please refer to the *STR73x Reference Manual*.

6.6 Power supplies

Power to the board is supplied using a lump in cord power supply providing 5 V to the board. For more details, refer to *Section 1: Power management*.

6.7 CAN interface

A general purpose, asynchronous serial I/O data port connected through a 9-pin D-type male connector with micro switches selectable between High or Low bus output S702, and between Standby or Slope control S50.

For more details, refer to the *CAN transceiver L9616 datasheet*.

6.8 RS232 serial interface

A general purpose, asynchronous serial I/O data port connected through a 9-pin D-type male connector.

RS232 connects directly to UART0, transmit and receive only (null modem).

RTS is shorted to CTS and DTR is shorted to DSR at the connector.

For more details, refer to the *RS232 transceiver ST3232 datasheet*.

6.9 Serial ROM

6.9.1 SPI EEPROM

8 Kbit SPI serial EEPROM connected to the buffered serial peripheral interface (BSPI). Switch S41 is used to enable or disable write protect (pull down = Write protect, pull up = Write enabled).

For more details, refer to the *SPI EEPROM M95080 datasheet*.

6.9.2 I2C EEPROM:

8 Kbit EEPROM connected to the I2C0 interface, Switch S40 is used to enable or disable write protect (pull down = Write protect, pull up = Write enabled).

For more details, refer to the *I2C EEPROM M24C08 datasheet*.

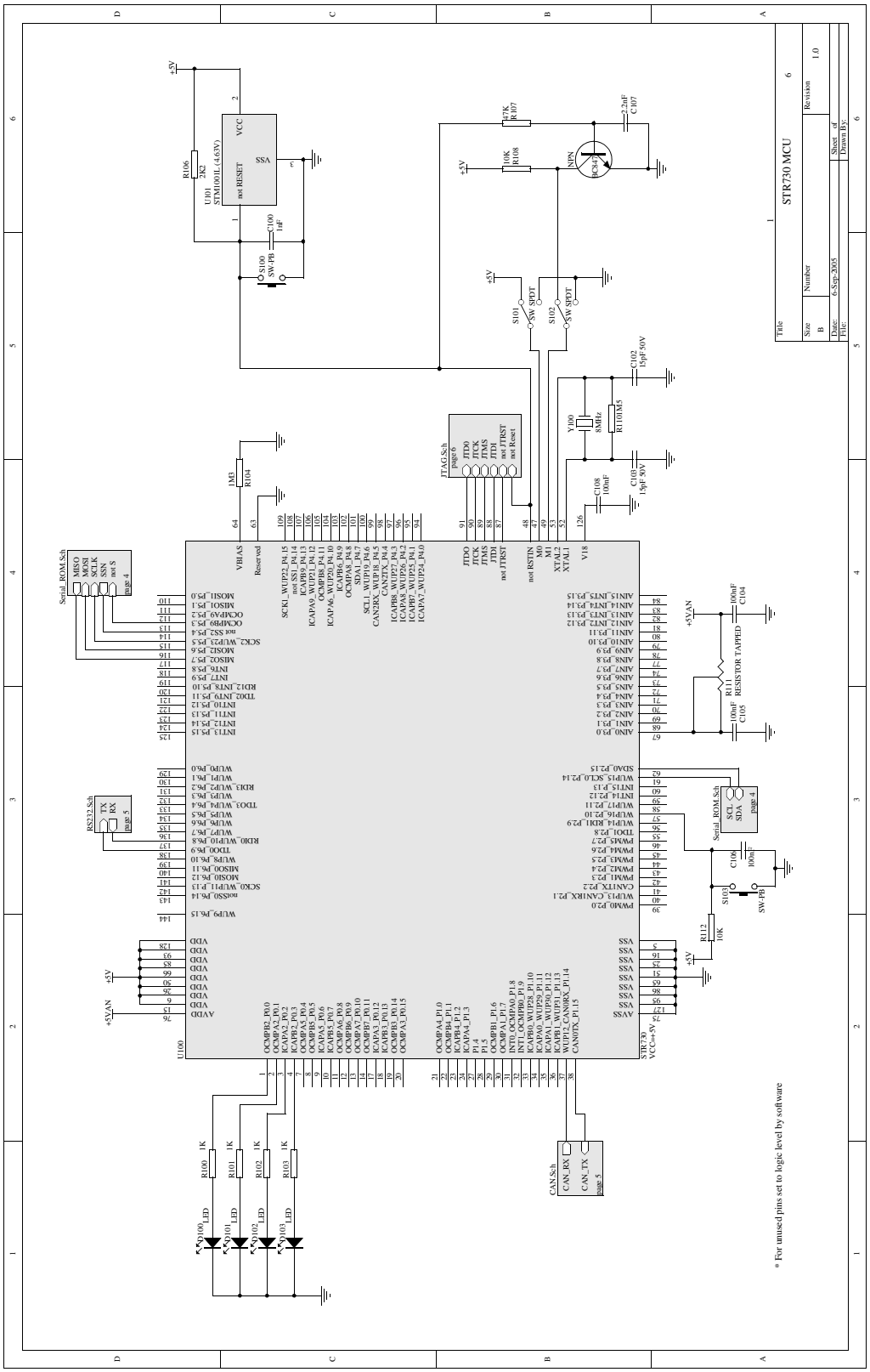
The values R43 and R45 depend essentially on the I2C communication speed.

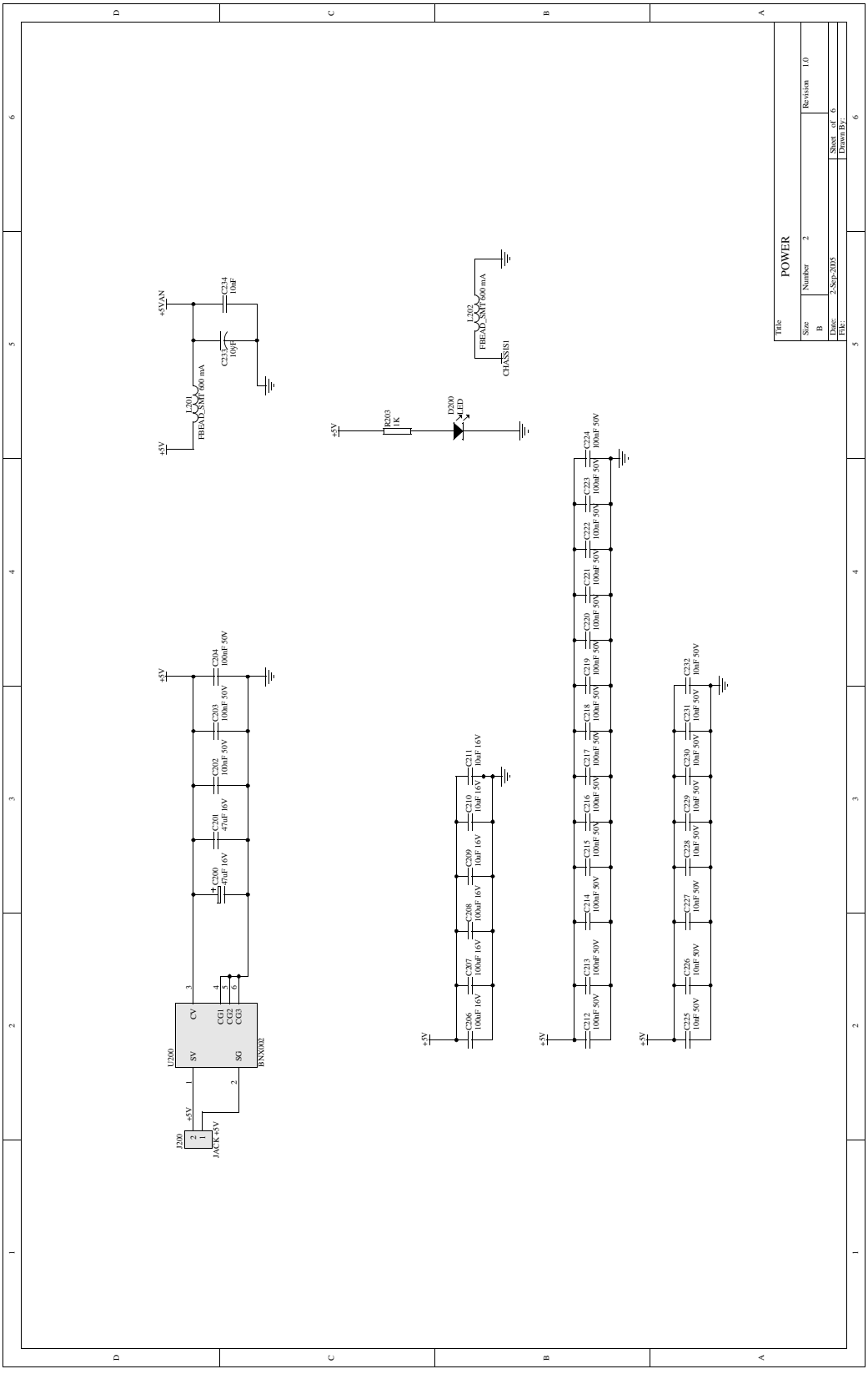
For more details on theses values, please refer to the *STR73x Reference Manual*.

6.10 JTAG interface

Refer to the *Section 5: Debug management*.

7 Schematics

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C200 47uF 16V
U200 5V CV SG CG1 CG2 CG3 BNX002
J200 JACK+5V
C211 10uF 16V
C210 10uF 16V
C209 10uF 16V
C208 10uF 16V
C207 10uF 16V
C206 10uF 16V
C224 100nF 50V
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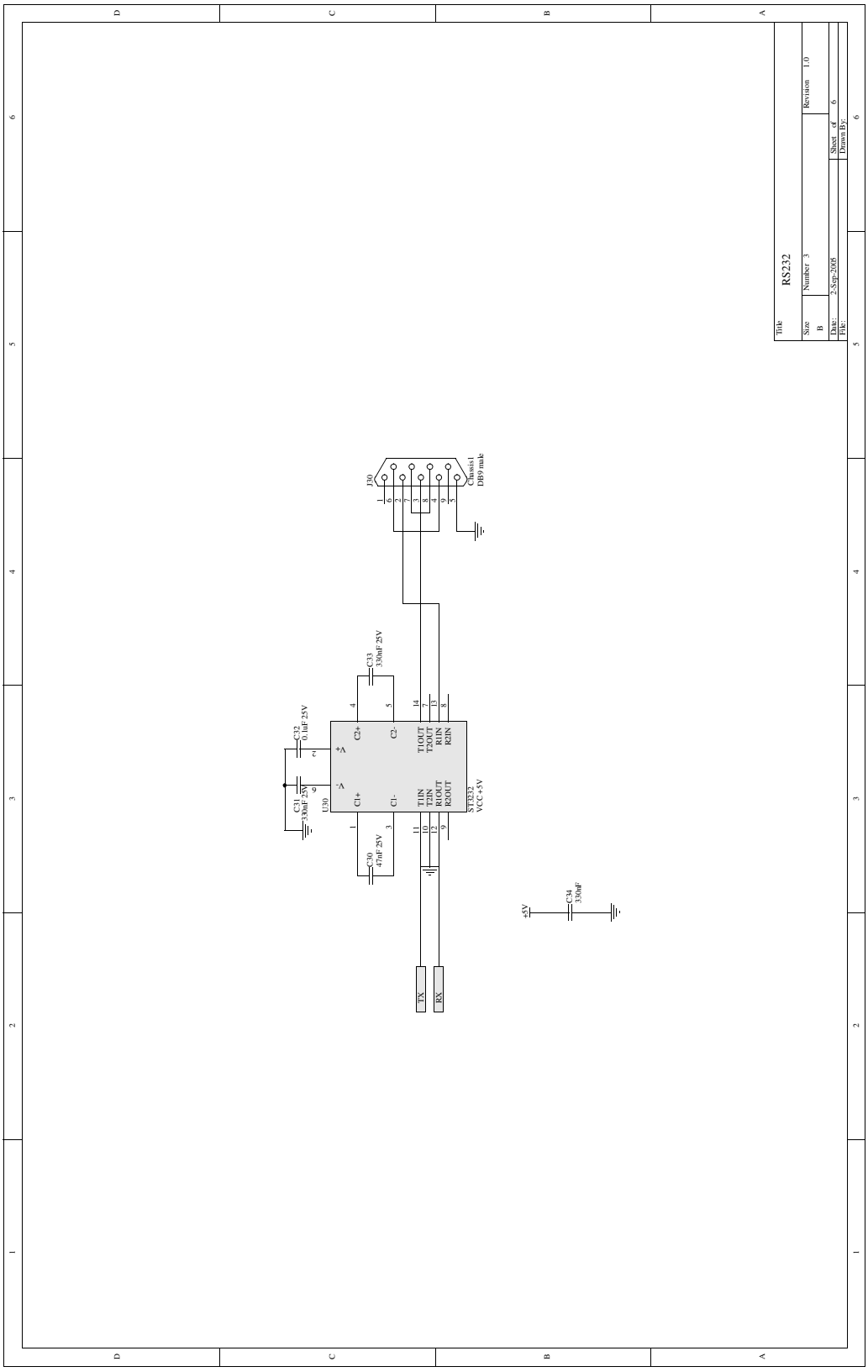
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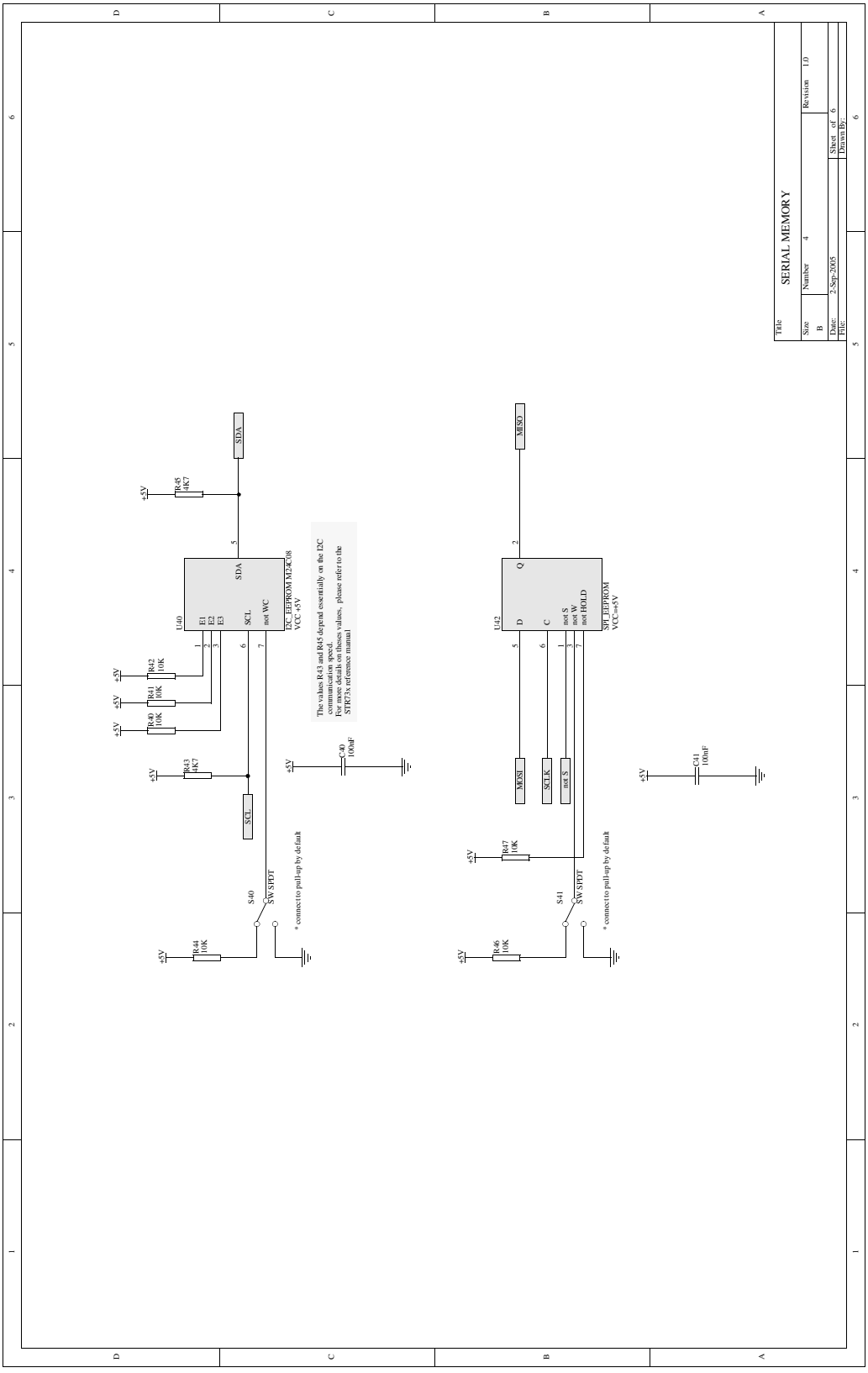
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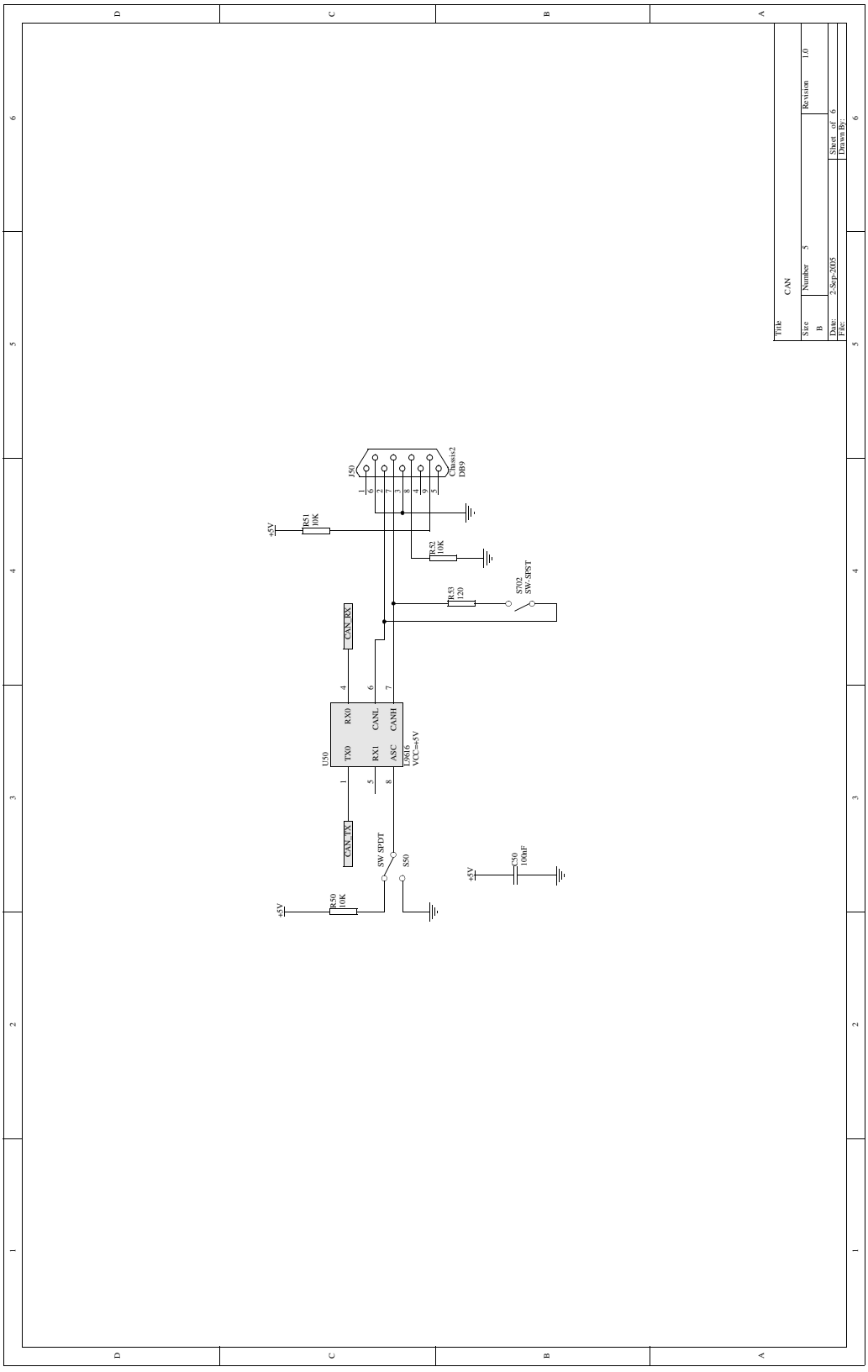
R42 10K
R41 10K
R40 10K
R43 4K7
R44 10K
R47 10K
R46 10K
C40 100nF
C41 100nF
S40
S41
SW SPDT
* connect to pull-up by default
U40
E1
E2
E3
not WC
I2C_EEPROM M24C08
VCC +5V
U42
D
Q
C
not S
not W
not HOLD
SPI_EEPROM
VCC=+5V
The values R43 and R45 depend essentially on the I2C communication speed.
For more details on theses values, please refer to the STR73x reference manual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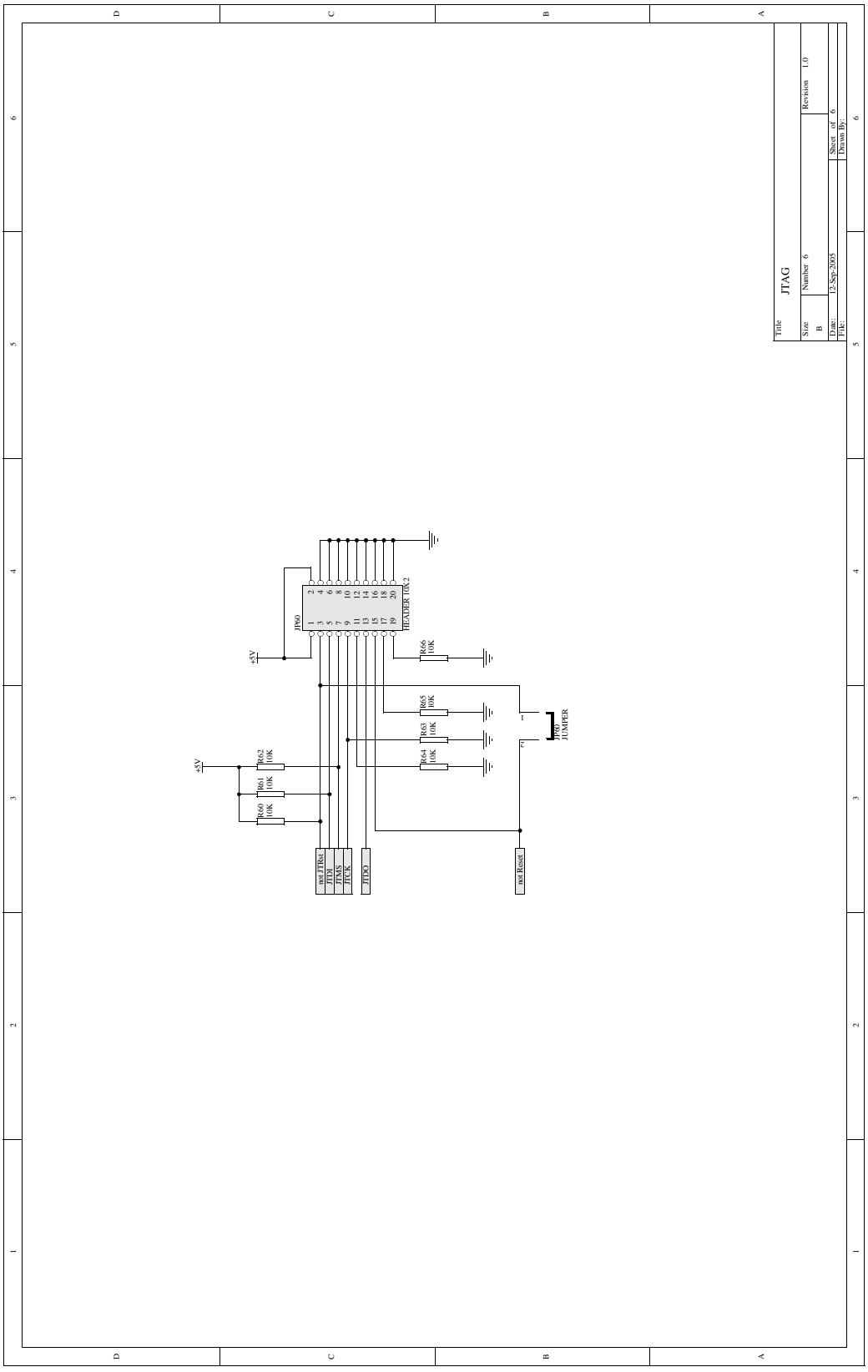
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R65 10K
R63 10K
R64 10K
R62 10K
R61 10K
R60 10K
JUMPER
not JTRst
JTDI
JTMS
JTCK
JTDO
not Reset

8 Revision history

Date	Revision	Changes
23-Sep-2005	1	Initial release