AN4075
Application note

STEVAL-IFP016V2 IO-Link communication master transceiver demonstration board

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Introduction

The STEVAL-IFP016V2 demonstration board works as an IO-Link communication master transceiver. In combination with the STEVAL-PCC009V2 or STEVAL-PCC009V1 demonstration board, the application can evaluate all the features of the L6360 IC.

The L6360 is a monolithic IO-Link master port, compliant with PHY2 (3 wires) supporting COM1 (4.8 kbaud), COM2 (38.4 kbaud) and COM3 (230.4 kbaud) modes.

The C/Q_O output stage (high-side, low-side or push-pull) as well as the cutoff current, cutoff current delay time, and restart delay are programmable.

The cutoff current and cutoff current delay time, combined with the thermal shutdown and automatic restart, protect the device against overload and short-circuit.

The C/Q_O and L+ output stages are able to drive resistive, inductive and capacitive loads. Fast demagnetization on the L+ switch is able to dissipate the energy stored in the inductive loads.

The supply voltage is monitored and low-voltage conditions are detected.

The L6360 transfers, through PHY2 (C/Q_O pin), data received from a host microcontroller to USART (INC/Q_O pin), or transfers data received from PHY2 (C/Q_I pin) to USART ($OUTC/Q_I$ pin). For more details on the complete system please refer to the application schematic.

To enable full IC control, configuration and monitoring (i.e. fault conditions stored in the status register), the communication between the system microcontroller and the L6360 is based on a fast mode, 2-wire I^2C bus.

The L6360 has 9 registers to manage the programmable parameters and the status of the IC.

Monitored fault conditions include L+ line, overtemperature, C/Q overload, linear regulator undervoltage, and parity check.

Internal LED driver circuitries, in open-drain configuration, provide two programmable sequences to drive two LEDs.

A large GND area on the printed circuit board has been designed in order to minimize noise and ensure good thermal performance.

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1 Features

- Supply voltage from 18 to 32.5 V
- Fully protected, programmable output stages
- Supports COM1, COM2 and COM3 mode
- 5 mA IO-Link digital input
- Additional IEC61131-2 type-1 input
- 3.3 V / 5 V, 50 mA linear regulator
- Fast mode I^2C for IC control, configuration and diagnostic
- Diagnostic dual-LED sequence generator and driver
- 5 V and 3.3 V compatible I/Os
- Interface compatible with STEVAL-PCC009V2 and STEVAL-PCC009V1
- EMC-immune application against ESD, burst, surge, RF noise, etc. according to IEC61000-4-2, IEC61000-4-4, IEC61000-4-5, IEC61000-4-6 standards

2 Board description

The STEVAL-IFP016V2 has external connectors for the supply voltage, two outputs (C/Q and L+), one input (I/Q) and a 30-pin connector to control and program the main functions of the board through an external demonstration board (STEVAL-PCC009V2 or STEVAL-PCC009V1).

Figure 1. STEVAL-IFP016V2 demonstration board

Table 1. STEVAL-IFP016V2 connector and jumper description

Name	Type	Function
INTERFACE1	30-pin connector	Communication with interface board
CON1	Power supply	Board power supply
CON2	Power outputs	C/Q, I/Q, L+, L- power outputs
J1	Jumper	$EN_{C/Q}$
J2	Jumper	EN_{L+}
J3	Jumper	I^2C address SA1
J4	Jumper	V_{CC} connected to V_H
J5	Jumper	I^2C address SA0
J6	Jumper	Linear regulator output voltage
J7	Jumper	I^2C address SA2
J8	Jumper	I^2C data bus SDA
J9	Jumper	I^2C clock bus SCL

Table 2. STEVAL-IFP016V2 30-pin signal connector description

Pin number	Description
2	GND
5	$IN_{C/Q}$
6	$OUT_{C/Q}$
9	SA1
10	SA2
11	SCL
12	SDA
15	EN_{L+}
16	$OUT_{I/Q}$
17	IRQ
18	RST
26	$EN_{C/Q}$
27	SA0
Others	Not connected

Table 3. STEVAL-IFP016V2 electrical specifications (recommended values)

Parameter	Value
Supply voltage range (V_S)	18 to 32.5 V
Logic input voltage range	0 to +5 V
Operating temperature range	-25 °C to +125 °C
L6360 thermal resistance junction-to-ambient	50 °C/W

Figure 2. STEVAL-IFP016V2 electrical schematic

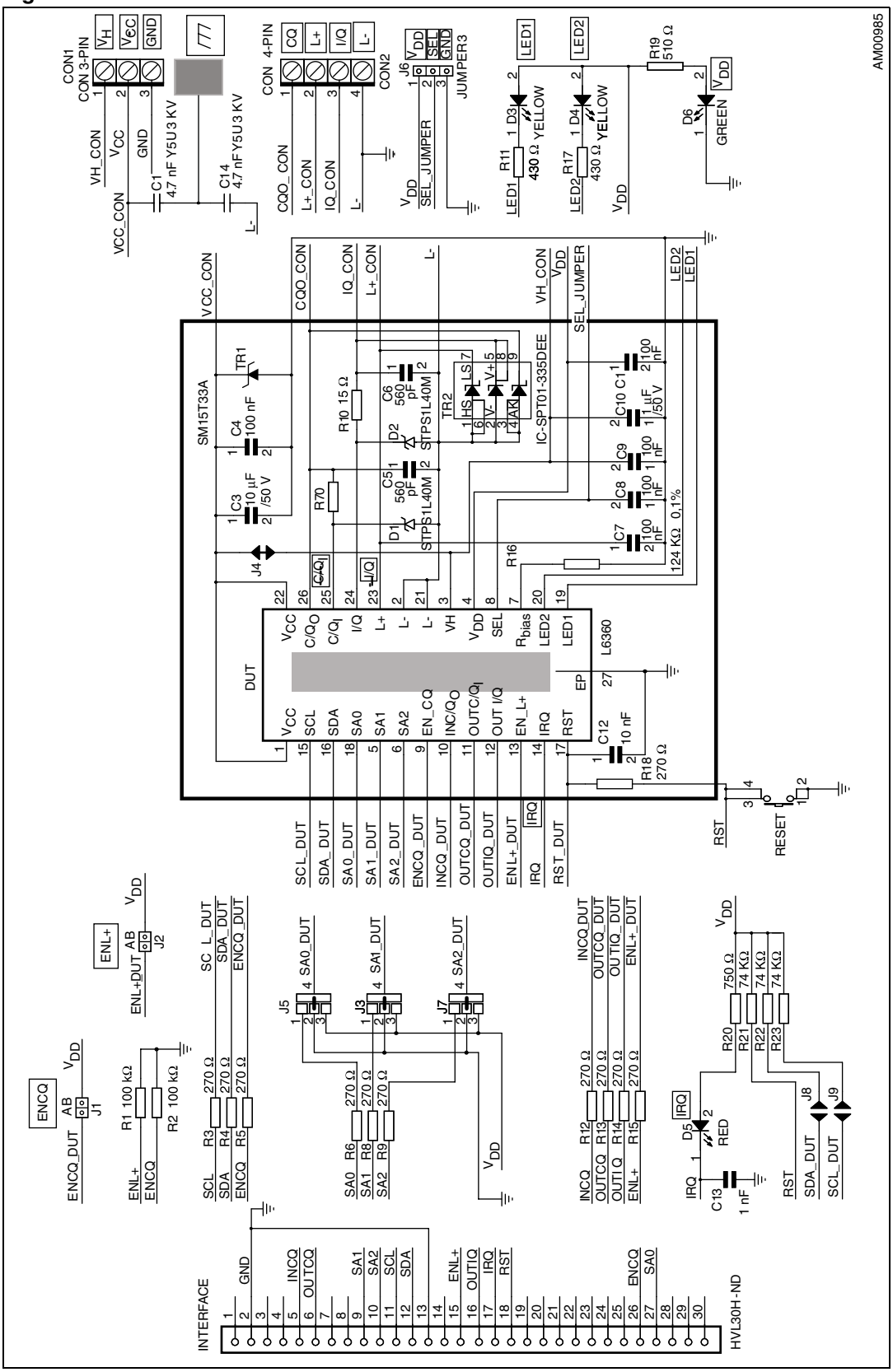


Table 4. STEVAL-IFP016V2 component list

Part reference	Part value	Part description
C1	4.7 nF	Y5U capacitor
C3	10 µF - 50 V	Ceramic capacitor
C4	100 nF	Ceramic capacitor
C5	560 pF	Ceramic capacitor
C6	560 pF	Ceramic capacitor
C7	100 nF	Ceramic capacitor
C8	100 nF	Ceramic capacitor
C9	100 nF	Ceramic capacitor
C10	1 µF - 50 V	Ceramic capacitor
C11	100 nF	Ceramic capacitor
C12	10 nF	Ceramic capacitor
C13	1 nF	Ceramic capacitor
C14	4.7 nF	Y5U capacitor
TR1	SM15T33A	Unidirectional Transil™
TR2	SPT01-335DEE	Triple Transil
D1	STPS1L40M	Schottky diode
D2	STPS1L40M	Schottky diode
D3		LED - yellow
D4		LED - yellow
D5		LED - red
D6		LED - green
R1	100 kΩ	Resistor
R2	100 kΩ	Resistor
R3	270 Ω	Resistor
R4	270 Ω	Resistor
R5	270 Ω	Resistor
R6	270 Ω	Trimmer
R7	0 Ω	
R8	270 Ω	Resistor
R9	270 Ω	Resistor
R10	15 Ω	Resistor
R11	430 Ω	Resistor
R12	270 Ω	Resistor
R13	270 Ω	Resistor
R14	270 Ω	Resistor

Table 4. STEVAL-IFP016V2 component list (continued)

Part reference	Part value	Part description
R15	270 Ω	Resistor
R16	100 k Ω - 1%	Resistor
R17	430 Ω	Resistor
R18	270 Ω	Resistor
R19	510 Ω	Resistor
R20	750 Ω	Resistor
R21	4.7 kΩ	Resistor
R22	4.7 kΩ	Resistor
R23	4.7 kΩ	Resistor
U1	L6360	IO-Link communication master transceiver

Figure 3. STEVAL-IFP016V2 component placement

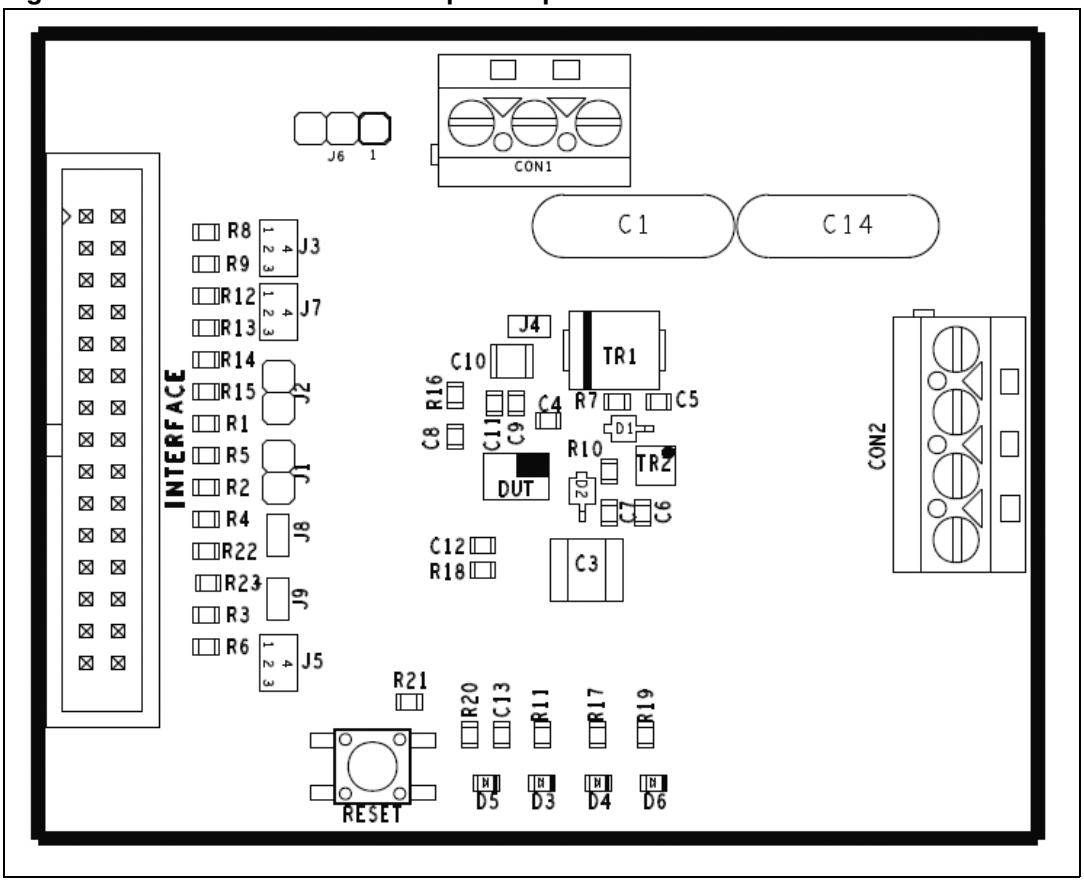


Figure 4. STEVAL-IFP016V2 topside layer

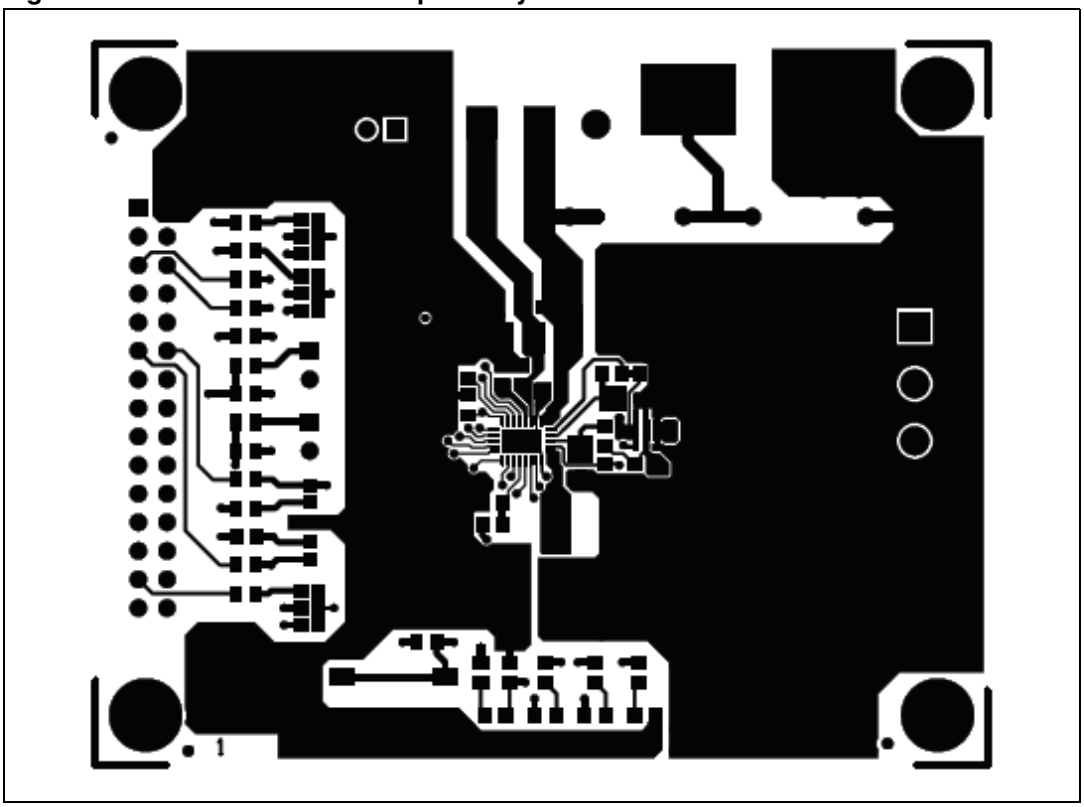


Figure 5. STEVAL-IFP016V2 inner 1st layer

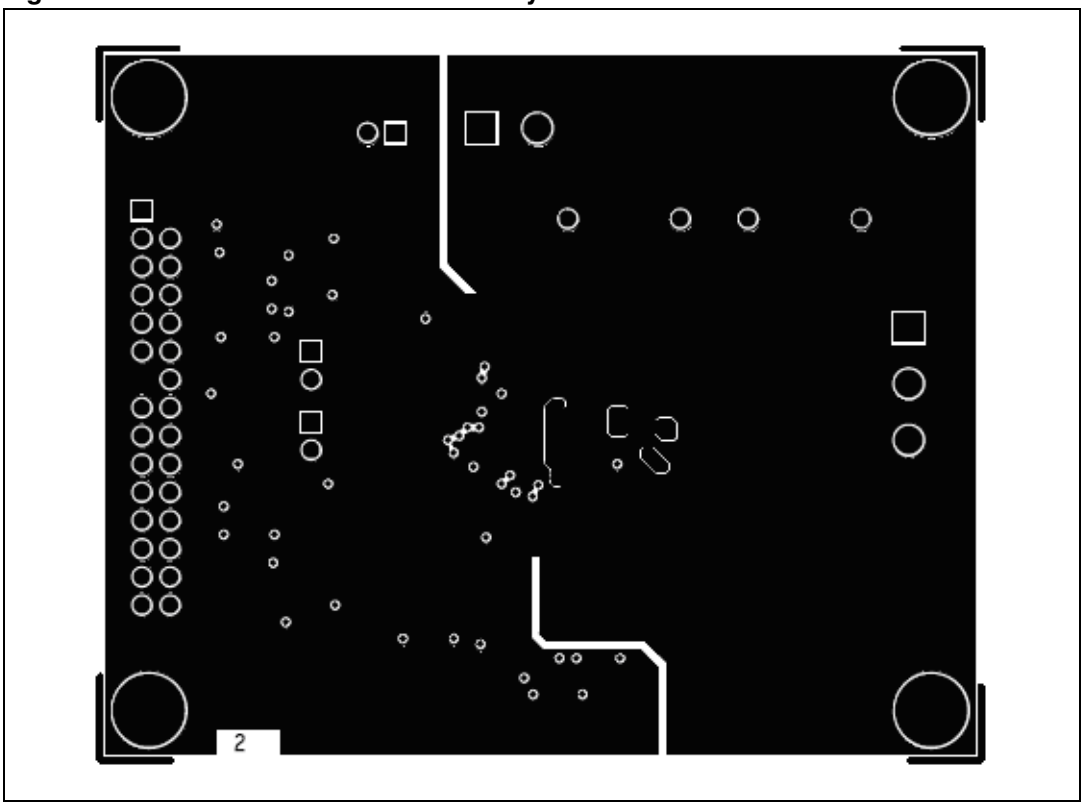


Figure 6. STEVAL-IFP016V2 inner 2nd layer

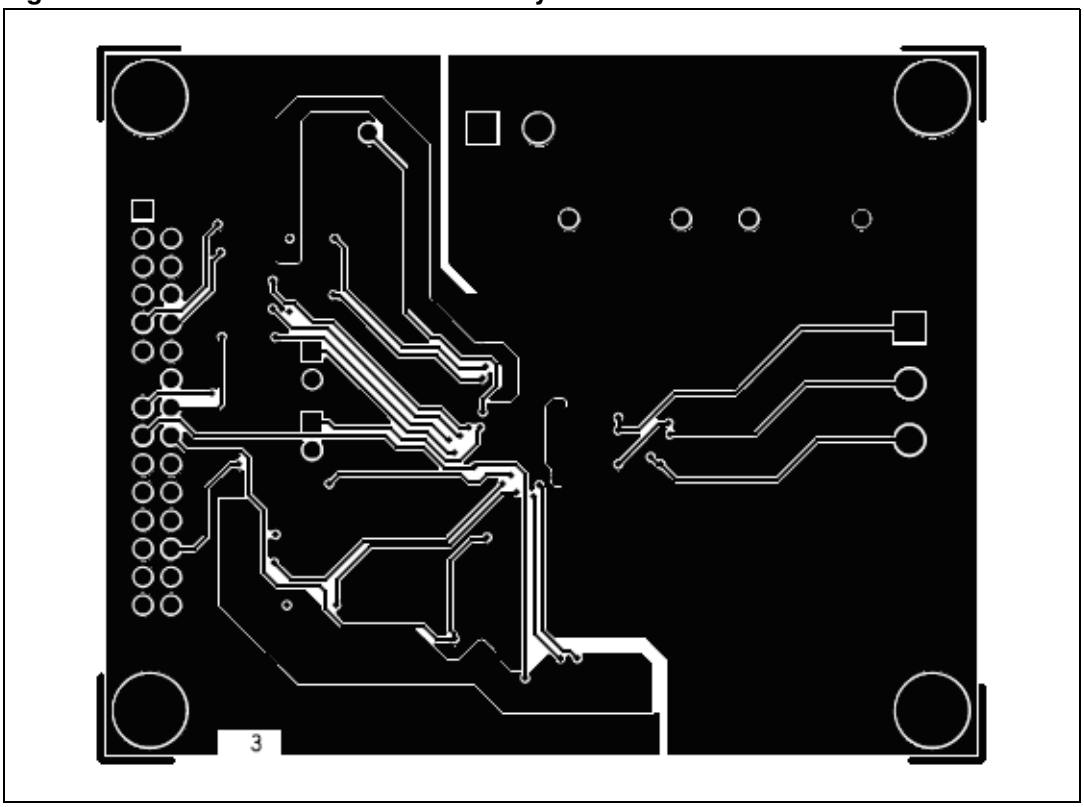
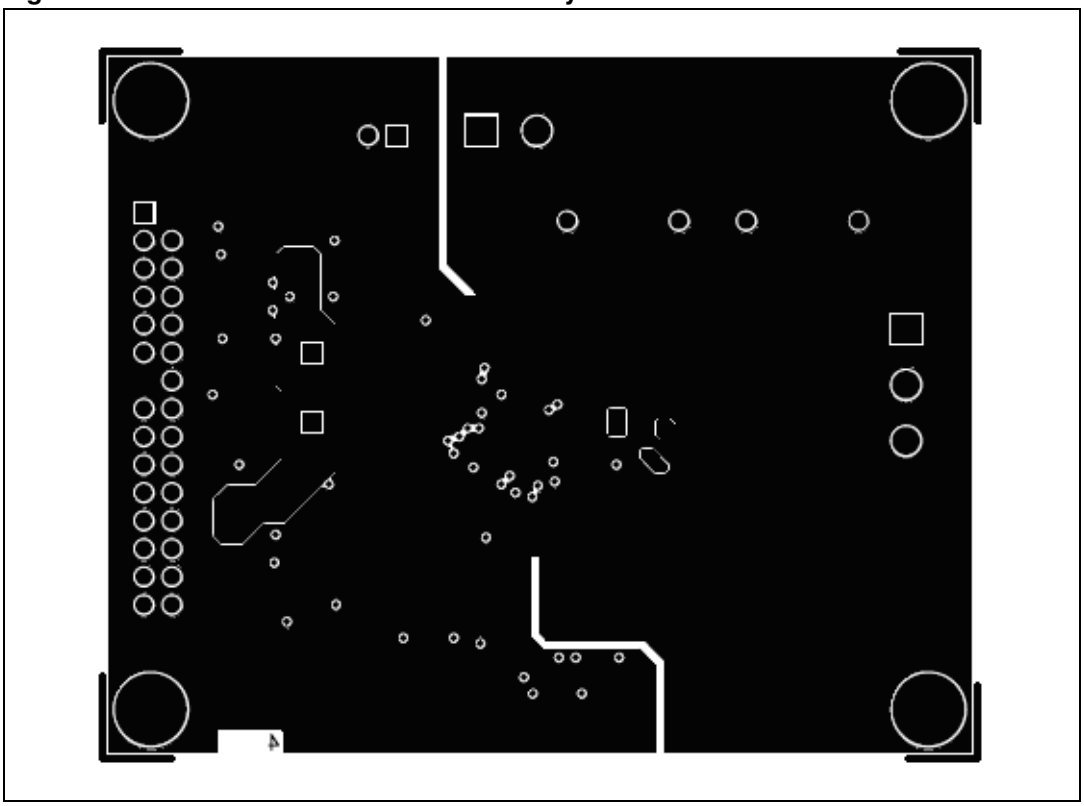


Figure 7. STEVAL-IFP016V2 bottomside layer



3 Using STEVAL-IFP016V2

The STEVAL-IFP016V2 board can be used in combination with the STEVAL-PCC009V2 or STEVAL-PCC009V1 demonstration board.

IC inputs can be controlled by the STEVAL-PCC009V2/1 or set by the hardware using jumpers on the board.

The CON1 connector is used to supply the board. Supply voltage should be connected to the V_{CC} pin. Linear regulator input voltage V_H can be connected directly to V_{CC} using jumper J4. If J4 is open, the V_H voltage must be kept below the V_{CC} value.

The 3.3 V or 5 V voltage for logic inputs and for the reference voltage is obtained from the linear regulator output V_{DD}. It is possible to select 3.3 V or 5 V using jumper J6.

Jumpers J3, J5 and J7 allow I^2C interface address configuration.

CON2 is used to provide input/output voltages from/to external circuits. The C/Q channel is used for communication (transceiver line), L+ is used to supply an IO-Link device, L- is shorted to GND and the I/Q channel is used as an additional input (communication) line.

3.1 Connection to the STEVAL-PCC009V2 or STEVAL-PCC009V1 demonstration board

The complete evaluation kit, apart from STEVAL-IFP016V2 also in the communication board, is used to program the IC and to control UART communication.

A GUI interface is used to configure the L6360 IC through the communication board.

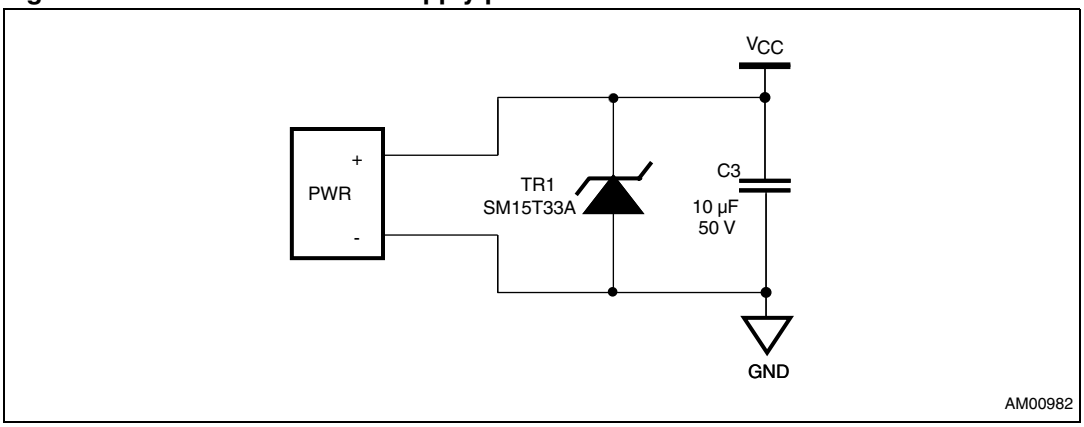
3.2 Basic supply protection circuit

A cost-effective supply voltage protection has been implemented, while reverse-polarity protection has not.

Supply overvoltage protection is provided by the **TR1** diode. It works as a primary overvoltage clamp to limit supply line distortions - like surge pulses or oscillations caused by line parasitic parameters (inductance) during the plug-in phase, for example. The rating of 1500 W is recommended to provide reliable protection. A unidirectional Transil must be used to avoid negative stress on the L6360.

An energy buffer filters the application supply to avoid high ripple during power driver switching, etc. **C3** is used as the filtering bulk capacitor.

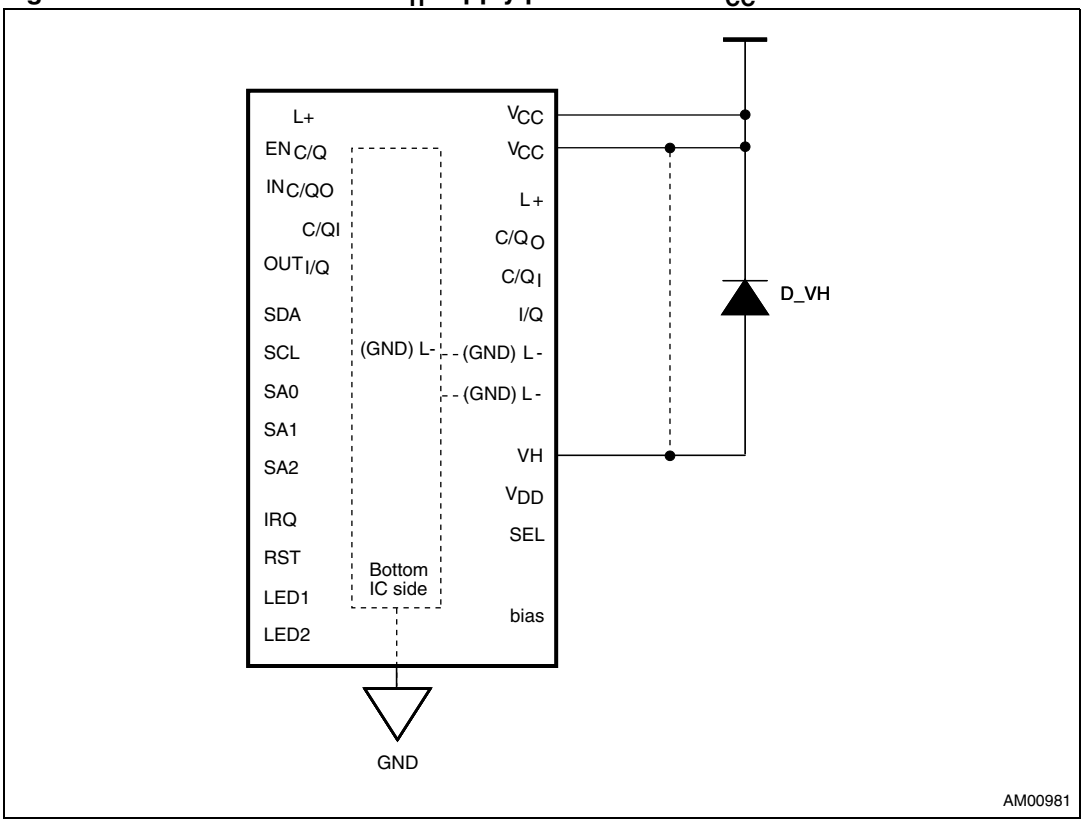
Figure 8. STEVAL-IFP016V2 supply protection



3.3 Independent V_H pin supply vs. direct connection to V_{CC}

V_H voltage must be always lower than (or equal to) V_{CC}, even during power-up and power-down of the application. Care must be taken when supplying V_H from another source (V_{CC} and V_H not connected together). In some cases a diode **D_VH** placed between V_{CC} and V_H may help to avoid this violation.

Figure 9. STEVAL-IFP016V2 V_H supply protection vs. V_{CC}



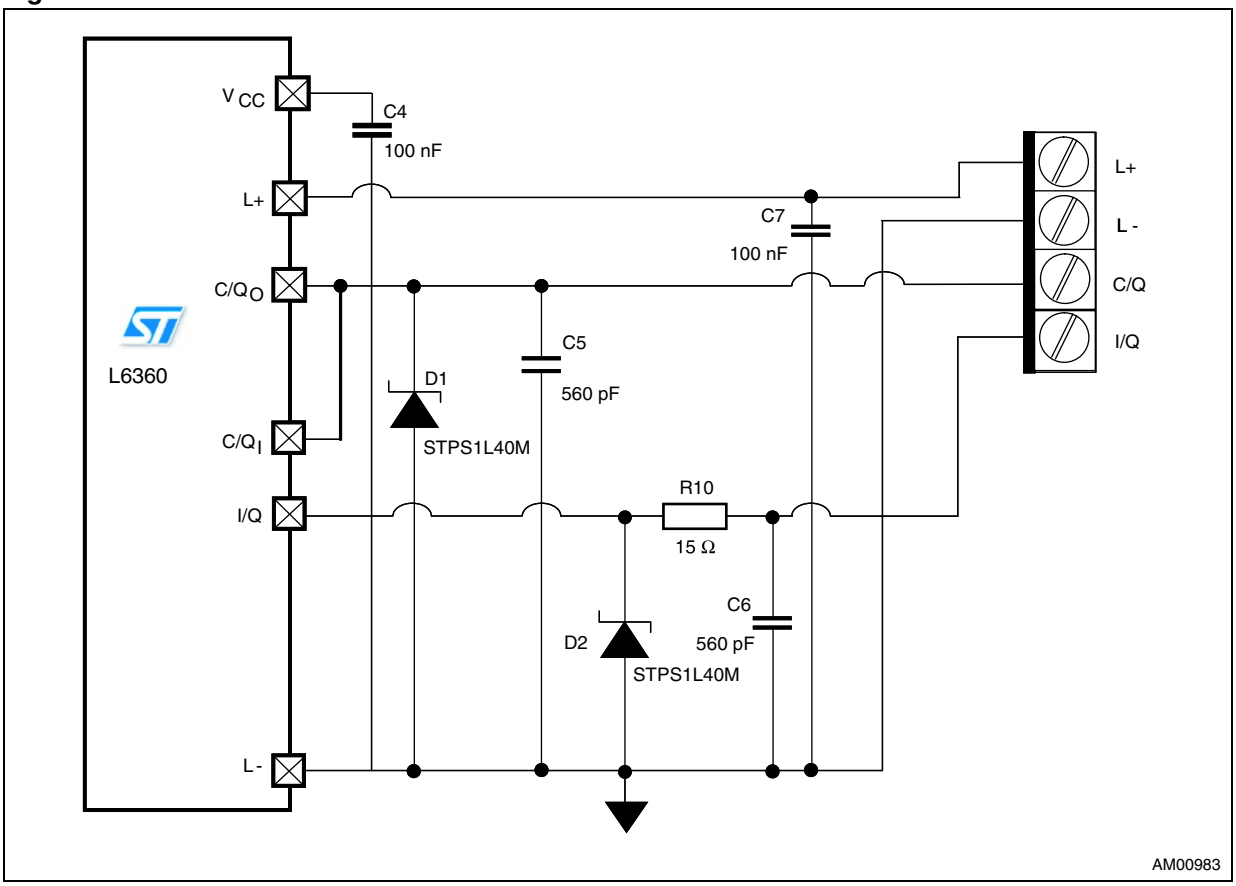
3.4 IO-Link communication

This section gives information about the implementation of a possible alternative I/O filter conforming only to the IO-Link standard. The board implements more advanced I/O protection circuitry (see *Section 4*).

An energy buffer for the L6360 supply makes the IC supply voltage stable and limits EMI noise. **C1** is used to block the power supply.

Capacitors **C5**, **C6**, **C7** work as a basic protection against fast transient signals like burst or a radio-frequency domain applied to the lines.

Figure 10. L6360 communication interface suitable for IO-Link



3.5 Standard IO (SIO) protection circuit

An energy buffer for the L6360 supply makes the IC supply voltage stable and limits EMI noise. **C4** is used to block the power supply.

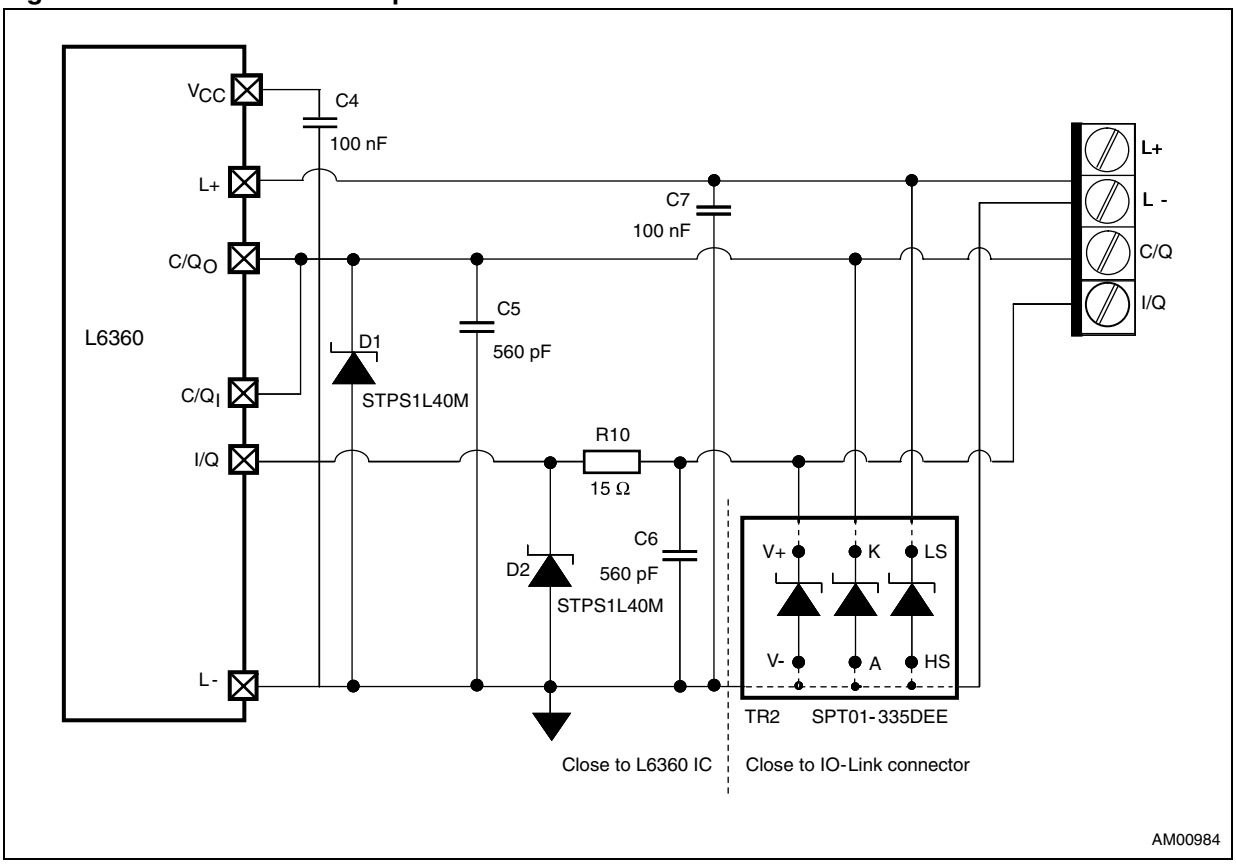
Capacitors **C5**, **C6**, **C7** work as a basic protection against fast transient signals like burst or a radio-frequency domain applied to the lines.

Schottky diodes with low V_F **D1** and **D2** are used for the suppression of negative voltage spikes. They clamp the disturbances applied to the lines in a reverse-polarity direction. Diodes can conduct high surge current pulses to avoid high peak current flow through the pins of the L6360 which could become damaged.

R10 is used to limit surge current. It reduces the current flow in the L6360 - I/Q pin in both polarities when surge pulses are applied to the line. If this resistor is omitted, the I/Q line surge immunity is lower.

Triple Transil **TR2** (**SPT01-335DEE**) is used as the primary surge protection to avoid overvoltage on the L6360 interface. It protects the L+ switch against negative voltage pulses, shares current flow of negative surge pulses with the additional Schottky diodes on the C/Q and I/Q lines, and clamps positive surge pulses applied to the C/Q and I/Q lines.

Figure 11. STEVAL-IFP016V2 protection circuit



4 Application EMC immunity

This paragraphs lists the STEVAL-IFP016V2 application EMC test results. The indicated immunity is considered as quantitative information only.

4.1 Register values

The L6360 has been initialized with the following configuration values:

- Configuration = 0 x 60 (push-pull)
- Control1 = 0 x F8
  - C/Q_I pull-down enabled
  - C/Q_O cutoff current = 500 mA
  - C/Q_O cutoff current delay = 250 µs
  - C/Q_O restart delay = 256 x 250 µs
  - C/Q_I debounce time (filter) is off (0 µs)
- Control2 = 0 x A0
  - I/Q pull-down enabled
  - C/Q_I pull-down generator 5.5 mA
  - L+ cutoff enabled
  - L+ cutoff delay 500 µs
  - L+ restart delay 64 ms
  - I/Q debounce time (filter) is off (0 µs)
- LED1H = 0 x 55 (highest blinking frequency)
- LED1L = 0 x 55
- LED2H = 0 X FF (lowest blinking frequency)
- LED2L = 0 x 00

4.2 Burst test

4.2.1 Test conditions

- Supply voltage: 23 VDC
- L+ switch ON (active), C/Q in Rx mode (PP but EN C/Q low)
- Register values - see *Section 4.1*
- L+, C/Q, I/Q lines loaded by 1 kΩ resistors vs. L-

4.2.2 Test signal

According the IEC 61000-4-4

- Polarity: positive/negative
- Burst duration: 15 ms ± 20% at 5 kHz
- Burst period: 300 ms ± 20%
- Duration time: 1 minute
- Applied to: L+, C/Q, I/Q and L- lines through capacitive clamp

4.2.3 Test setup

The EFT signal was coupled to the supply voltage lines through the capacitive coupling clamp which corresponds to approximately 150 pF.

The application supply voltage was provided by two 12 V lead battery cells.

Earth (reference plain) was connected to the application.

Table 5. Application EFT (burst) immunity, applied to IO-Link lines (L+, C/Q, I/Q, L-)

Polarity	EFT test signal amplitude, test result			
	1 kV	2 kV	3 kV	4 kV
Positive (+)	A(1)	A(1)	A(1)	A(1)
Negative (-)	A(1)	A(1)	A(1)	A(1)

1. The L6360 internal registers state stable; logic interface state changes not evaluated.

4.2.4 Conclusion

The application is immune against fast transient burst signals.

Burst applied to the IO-Link communication lines has no influence on the stability of the L6360 internal registers.

4.3 EMC IEC 61000-4-5 surge immunity test

4.3.1 Test conditions

- Supply voltage: 23 V (approximately)
- Ambient temperature: 23 °C
- L+, C/Q configured as mentioned in *Table 6* to *Table 8*
- Register values - see *Section 4.1*
- L+, C/Q, I/Q lines left floating

4.3.2 Test signal

According to IEC 61000-4-5:

- 5 positive and 5 negative surges
- Repetition rate: 1 min.
- Coupling: 42 Ω/0.5 µF
- Applied to:
  - IO-Link bus lines (L+, C/Q and I/Q) - common/differential mode
  - Supply lines (V_{CC}, GND) - common/differential mode

4.3.3 Test setup

The test was executed on the IO-Link bus lines (L+, C/Q and I/Q vs. earth reference).

Tests were made on the output lines vs. earth - common mode (CM), as well as on output lines vs. L- (GND) - in differential mode. The earth reference is coupled by 2 x 4.7 nF/3 kV capacitors (C1, C14) with V_{CC} and GND. The length of the cables was minimized. The surge pulse was coupled with a coupling network of 42 Ω/0.5 µF.

After every surge sequence, the power supply current and C/Q, I/Q current sink values were measured and compared to their initial state and the functionality of the receiver and driver paths (functionality of the output switches) was checked.

4.3.4 Test results

Table 6. Application surge immunity - common mode

Surge test signal amplitude, test result at polarity (+ / -)					
Applied to	**500 V**	**1 kV**	**1.5 kV**	**2 kV**	**2.5 kV**
L+ OFF	- / -	A(1) / A(1)	A(1) / A(1)	A(1) / A(1)	A(1) / A(1)
L+ ON	A(1) / A(1)	A(1) / A(1)	A(1) / A(1)	A(1) / A(1)	A(1) / A(1)
C/Q LS ON	A(1) / A(1)	A(1) / A(1)	A(1) / A(1)	A(1) / A(1)	A(1) / A(1)
C/Q HS ON	A(1) / A(1)	A(1) / A(1)	A(1) / A(1)	A(1) / A(1)	A(1) / A(1)
C/Q Rx mode	A(1) / A(1)	A(1) / A(1)	A(1) / A(1)	A(1) / A(1)	A(1) / A(1)
I/Q	- / -	A(1) / A(1)	A(1) / A(1)	A(1) / A(1)	A(1) / A(1)

1. The values of the L6360 internal registers did not change.

Table 7. Application surge immunity - differential mode

Surge test signal amplitude, test result at polarity (+ / -)					
Applied to	**500 V**	**1 kV**	**1.5 kV**	**2 kV**	**2.5 kV**
L+ OFF	A(1) / A(1)	A(1)/ A(1)	- / -	- / -	- / -
L+ ON	A(1)/ B(2)	B(2) / B(2)	- / -	- / -	- / -
C/Q LS ON	A(1)/ A(1)	A(1) / B(2)	- / -	- / -	- / -
C/Q HS ON	A(1)/ A(1)	A(1) / B(2)	- / -	- / -	- / -
C/Q Rx mode	A(1) / B(2)	B(2) / B(2)	- / -	- / -	- / -
I/Q	A(1)/ A(1)	A(1)/ A(1)	- / -	- / -	- / -

1. The values of the L6360 internal registers did not change.
2. The L6360 registers were reset, IRQ signal is activated.

Table 8. Application supply surge immunity CM, DM

Surge test signal amplitude, test result at polarity (+ / -)					
Applied to:	**500 V**	**1 kV**	**1.5 kV**	**2 kV**	**2.5 kV**
V_{CC} vs. earth (CM)	- / -	- / -	- / -	- / -	$A^{(1)}$ / $A^{(1)}$
V_{CC}vs L- (DM)	$A^{(1)}$ / $B^{(2)}$	$B^{(2)}$ / $B^{(2)}$	$B^{(2)}$ / $B^{(2)}$	$B^{(2)}$ / $B^{(2)}$	$B^{(2)}$ / $B^{(2)}$

1. The values of the L6360 internal registers did not change.
2. The L6360 registers were reset and IRQ signal activated.

4.3.5 Conclusion

Immunity of different L6360 pins was evaluated and the external protection circuit adjusted accordingly. The protection circuit which showed the best EMC performance is used in the STEVAL-IFP016V2 application.

C/Q transceiver

The **C/Q_I** and **C/Q_O** pins should be protected against negative overvoltages (higher than approximately 1.5 V) during the surge test. If the negative pulse is higher than the mentioned value, the internal structure can be damaged. It is recommended to short both pins together and protect them with a low V_F drop Schottky diode (e.g. STPS1L40), a 560 pF ceramic capacitor and one diode of SPT01-335DEE array.

I/Q receiver

The I/Q pin should be protected in a similar way against negative overvoltages. Tests showed positive immunity results when using an external low V_F Schottky diode (STPS1L40), a 15 Ω resistor in series, a 560 nF capacitor and one diode of SPT01-335DEE array. When a 15 Ω resistor is omitted, the chip fails at -2 kV CM surge pulse amplitude.

L+ driver

Protecting the L+ pin with a 100 nF ceramic capacitor and one diode of SPT01-335DEE array showed sufficient immunity against 2.5 kV CM / 1 kV DM surge pulses.

Supply (V_{CC}, L- / GND)

External protection circuits in the application provide sufficient immunity against surge pulses (CM/DM) applied to supply lines. Even 2.5 kV surge pulses did not cause degradation of the L6360 IC.

5 Revision history

Table 9. Document revision history

Date	Revision	Changes
25-Apr-2012	1	Initial release.