AN4654
Application note

Migrating between STM32L1 and STM32L0 series microcontrollers

Introduction

For designers of STM32 applications, it is important to be able to easily replace one microcontroller with another within the same product family.

One key advantage of STM32 MCUs is their simplified porting thanks to a strong focus on compatibility across the portfolio. Migrating an application to a different microcontroller is often needed to fulfill higher product requirements, more demanding on memory size or with increased number of I/Os. Cost reduction is another reason for change to smaller components and shrunk PCB area.

Table 1 lists the products addressed by this application note, prepared to help users during the analysis of the steps required to migrate from a STM32L1 microcontroller to one of the STM32L0 series. It gathers the most important information and lists the mandatory aspects that users need to address.

To migrate an application from STM32L1 series to STM32L0 series, users have to analyze the hardware migration first, then the peripheral migration and finally the firmware migration.

To fully benefit from the information included in this application note, users should be familiar with STM32 microcontrollers, and refer to the following documents available from *www.st.com*:

- STM32L1xx reference manual (RM0038) and product datasheets
- STM32L0xx reference manual (RM0367) and product datasheets.

For an overview of all the STM32 microcontrollers and for a comparison of the different features of each product series, please refer to AN3364 "*Migration and compatibility guidelines for STM32 microcontroller applications*."

Table 1. Applicable products

Type	Product series
Microcontrollers	STM32L0
	STM32L1

Note: The following notational convention is used in the rest of the document: STM32L0xx is used instead of STM32L0xxx when referring to products of STM32L0 series, and STM32L1xx is used instead of STM32L1xxx when referring to products of STM32L1 series.

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1 Hardware migration from the STM32L1 series to the STM32L0 series

The low-power STM32L1xx and STM32L0xx families are pin-to-pin compatible. All peripherals share the same pins on packages common to both families.

The transition from the STM32L1 series to the STM32L0 series is simple, the pinout summary for all common packages is detailed in *Table 2*.

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Table 2. STM32L1xx and STM32L0xx pinout summary

Pin name	STM32L1					STM32L0				
	LQFP48	LQFP64	BGA64	LQFP100	BGA100	LQFP48	LQFP64	BGA64	LQFP100	BGA100
PE2	-	-	-	1	B2	-	-	-	1	B2
PE3	-	-	-	2	A1	-	-	-	2	A1
PE4	-	-	-	3	B1	-	-	-	3	B1
PE5	-	-	-	4	C2	-	-	-	4	C2
PE6	-	-	-	5	D2	-	-	-	5	D2
VLCD	1	1	B2	6	E2	1	1	B2	6	E2
PC13 / ANTI_TAMP	2	2	A2	7	C1	2	2	A2	7	C1
PC14 / OSC32_IN	3	3	A1	8	D1	3	3	A1	8	D1
PC15 / OSC32_OUT	4	4	B1	9	E1	4	4	B1	9	E1
VSS_5	-	-	-	10	F2	-	-	-	10	F2
VDD_5	-	-	-	11	G2	-	-	-	11	G2
PH0 / OSC_IN	5	5	C1	12	F1	5	5	C1	12	F1
PH1 / OSC_OUT	6	6	D1	13	G1	6	6	D1	13	G1
NRST	7	7	E1	14	H2	7	7	E1	14	H2
PC0	-	8	E3	15	H1	-	8	E3	15	H1
PC1	-	9	E2	16	J2	-	9	E2	16	J2
PC2	-	10	F2	17	J3	-	10	F2	17	J3
PC3	-	11	-	18	K2	-	11	-	18	K2
VSSA	8	12	F1	19	J1	8	12	F1	19	J1
VREF-	-	-	-	20	K1	-	-	-	20	K1
VREF+	-	-	G1	21	L1	-	-	G1	21	L1
VDDA	9	13	H1	22	M1	9	13	H1	22	M1
PA0 / WKUP	10	14	G2	23	L2	10	14	G2	23	L2
PA1	11	15	H2	24	M2	11	15	H2	24	M2

Table 2. STM32L1xx and STM32L0xx pinout summary (continued)

Pin name	STM32L1					STM32L0				
	LQFP48	LQFP64	BGA64	LQFP100	BGA100	LQFP48	LQFP64	BGA64	LQFP100	BGA100
PA2	12	16	F3	25	K3	12	16	F3	25	K3
PA3	13	17	G3	26	L3	13	17	G3	26	L3
VSS_4	-	18	C2	27	E3	-	18	C2	27	E3
VDD_4	-	19	D2	28	H3	-	19	D2	28	H3
PA4	14	20	H3	29	M3	14	20	H3	29	M3
PA5	15	21	F4	30	K4	15	21	F4	30	K4
PA6	16	22	G4	31	L4	16	22	G4	31	L4
PA7	17	23	H4	32	M4	17	23	H4	32	M4
PC4	-	24	H5	33	K5	-	24	H5	33	K5
PC5	-	25	H6	34	L5	-	25	H6	34	L5
PB0	18	26	F5	35	M5	18	26	F5	35	M5
PB1	19	27	G5	36	M6	19	27	G5	36	M6
PB2	20	28	G6	37	L6	20	28	G6	37	L6
PE7	-	-	-	38	M7	-	-	-	38	M7
PE8	-	-	-	39	L7	-	-	-	39	L7
PE9	-	-	-	40	M8	-	-	-	40	M8
PE10	-	-	-	41	L8	-	-	-	41	L8
PE11	-	-	-	42	M9	-	-	-	42	M9
PE12	-	-	-	43	L9	-	-	-	43	L9
PE13	-	-	-	44	M10	-	-	-	44	M10
PE14	-	-	-	45	M11	-	-	-	45	M11
PE15	-	-	-	46	M12	-	-	-	46	M12
PB10	21	29	G7	47	L10	21	29	G7	47	L10
PB11	22	30	H7	48	L11	22	30	H7	48	L11
VSS_1	23	31	D6	49	F12	23	31	D6	49	F12
VDD_1	24	32	E5	50	G12	24	32	E5	50	G12
PB12	25	33	H8	51	L12	25	33	H8	51	L12
PB13	26	34	G8	52	K12	26	34	G8	52	K12
PB14	27	35	F8	53	K11	27	35	F8	53	K11
PB15	28	36	F7	54	K10	28	36	F7	54	K10
PD8	-	-	-	55	K9	-	-	-	55	K9

Table 2. STM32L1xx and STM32L0xx pinout summary (continued)

Pin name	STM32L1					STM32L0				
	LQFP48	LQFP64	BGA64	LQFP100	BGA100	LQFP48	LQFP64	BGA64	LQFP100	BGA100
PD9	-	-	-	56	K8	-	-	-	56	K8
PD10	-	-	-	57	J12	-	-	-	57	J12
PD11	-	-	-	58	J11	-	-	-	58	J11
PD12	-	-	-	59	J10	-	-	-	59	J10
PD13	-	-	-	60	H12	-	-	-	60	H12
PD14	-	-	-	61	H11	-	-	-	61	H11
PD15	-	-	-	62	H10	-	-	-	62	H10
PC6	-	37	F6	63	E12	-	37	F6	63	E12
PC7	-	38	E7	64	E11	-	38	E7	64	E11
PC8	-	39	E8	65	E10	-	39	E8	65	E10
PC9	-	40	D8	66	D12	-	40	D8	66	D12
PA8	29	41	D7	67	D11	29	41	D7	67	D11
PA9	30	42	C7	68	D10	30	42	C7	68	D10
PA10	31	43	C6	69	C12	31	43	C6	69	C12
PA11	32	44	C8	70	B12	32	44	C8	70	B12
PA12	33	45	B8	71	A12	33	45	B8	71	A12
PA13	34	46	A8	72	A11	34	46	A8	72	A11
PH2	-	-	-	73	C11	-	-	-	73	C11
VSS_2	35	47	D5	74	F11	35	47	D5	74	F11
VDD_2	36	48	E6	75	G11	36	48	E6	75	G11
PA14	37	49	A7	76	A10	37	49	A7	76	A10
PA15	38	50	A6	77	A9	38	50	A6	77	A9
PC10	-	51	B7	78	B11	-	51	B7	78	B11
PC11	-	52	B6	79	C10	-	52	B6	79	C10
PC12	-	53	C5	80	B10	-	53	C5	80	B10
PD0	-	-	-	81	C9	-	-	-	81	C9
PD1	-	-	-	82	B9	-	-	-	82	B9
PD2	-	54	B5	83	C8	-	54	B5	83	C8
PD3	-	-	-	84	B8	-	-	-	84	B8
PD4	-	-	-	85	B7	-	-	-	85	B7
PD5	-	-	-	86	A6	-	-	-	86	A6

Table 2. STM32L1xx and STM32L0xx pinout summary (continued)

Pin name	STM32L1					STM32L0				
	LQFP48	LQFP64	BGA64	LQFP100	BGA100	LQFP48	LQFP64	BGA64	LQFP100	BGA100
PD6	-	-	-	87	B6	-	-	-	87	B6
PD7	-	-	-	88	A5	-	-	-	88	A5
PB3	39	55	A5	89	A8	39	55	A5	89	A8
PB4	40	56	A4	90	A7	40	56	A4	90	A7
PB5	41	57	C4	91	C5	41	57	C4	91	C5
PB6	42	58	D3	92	B5	42	58	D3	92	B5
PB7	43	59	C3	93	B4	43	59	C3	93	B4
BOOT0	44	60	B4	94	A4	44	60	B4	94	A4
PB8	45	61	B3	95	A3	45	61	B3	95	A3
PB9	46	62	A3	96	B3	46	62	A3	96	B3
PE0	-	-	-	97	C3	-	-	-	97	C3
PE1	-	-	-	98	A2	-	-	-	98	A2
VSS_3	47	63	D4	99	D3	47	63	D4	99	D3
VDD_3	48	64	E4	100	C4	48	64	E4	100	C4

2 Boot mode compatibility

The way to select the boot mode on the STM32L0xx products differs from STM32L1xx product family. Instead of using two pins for the boot mode setting, STM32L0xx products use BOOT0 pin and retrieve the nBOOT1 value from an option bit located in the User option bytes at 0x1FF80000 memory address.

On the STM32L01x and STM32L02x devices the BOOT0 pin can be replaced by nBOOT0 bit using the BOOT_SEL bit in the User option bytes. This provides the ability to use the BOOT0 pin as GPIO input only pin on the device.

Table 3 summarizes the different configurations available for the Boot mode selection.

Table 3. Boot modes(1)

Boot mode configuration				Mode
n BOOT1 bit	BOOT0 pin	BOOT_SEL bit	nBOOT0 bit	
x	0	0	x	**Main Flash memory** is selected as boot space
1	1	0	x	**System memory** is selected as boot space
0	1	0	x	**Embedded SRAM** is selected as boot space
x	x	1	1	**Main Flash memory** is selected as boot space
1	x	1	0	**System memory** is selected as boot space
0	x	1	0	**Embedded SRAM** is selected as boot space

1. Gray options are available on STM32L01x and STM32L02x devices only.

Note: The BOOTx value is the opposite of the nBOOTx option bit, where x stands for 1 and 2.

3 Peripheral migration

As shown in *Table 4*, and further specified in *Section 3.1*, there are three categories of peripherals.

The common peripherals are supported with the dedicated firmware library without any modification, except if the peripheral instance is no longer present. You can change the instance and, of course, all the related features (clock configuration, pin configuration, interrupt/DMA request).

The modified peripherals such as ADC, RCC and I2C are different from the STM32L1 series ones and should be updated to take advantage of the enhancements and the new features in STM32L0 series.

All these modified peripherals in the STM32L0 series are enhanced to obtain smaller silicon print with features designed to offer advanced high-end capabilities in economical end products and to fix some limitations present in the STM32L1 series.

3.1 STM32 product cross-compatibility

The STM32 series embeds a set of peripherals which can be classed in three categories:

- The first category is for the peripherals which are, by definition, common to all products. Those peripherals are identical, so they have the same structure, registers and control bits. There is no need to perform any firmware change to keep the same functionality, at the application level, after migration. All the features and behavior remain the same.
- The second category is for the peripherals which are shared by all products but have only minor differences (in general to support new features). The migration from one product to another is very easy and does not need any significant new development effort.
- The third category is for peripherals which have been considerably changed from one product to another (new architecture, new features...). For this category of peripherals, the migration will require new development, at the application level.

Table 4 gives a general overview of this classification.

Table 4. STM32 peripheral compatibility analysis, STM32L1 vs. STM32L0 series(1)

Peripheral	STM32L1	STM32L0	Compatibility		
			Features	Pinout	Firmware
SPI	Yes	Yes	Same features	Identical + New GPIO added	Full compatibility
WWDG	Yes	Yes	Same features	NA	Full compatibility
IWDG	Yes	Yes++	Added a Window mode	NA	Partial compatibility
DBGMCU	Yes	Yes	No JTAG, No Trace	Identical for the SWD	Partial compatibility
CRC	Yes	Yes++	Added user polynomial, reverse capability and initial CRC value	NA	Partial compatibility

Table 4. STM32 peripheral compatibility analysis, STM32L1 vs. STM32L0 series(1) (continued)

Peripheral	STM32L1	STM32L0	Compatibility		
			Features	Pinout	Firmware
EXTI	Yes	Yes+	Some peripherals are able to generate event in Stop mode (direct event)	Identical	Full compatibility
DMA	Yes	Yes	Only 1 DMA controller with up to 7 channels (DMA2 not present)	NA	Partial compatibility
TIM	Yes	Yes	Different set of timers, similar functionality	Identical for the same timers (TIM2, TIM3, TIM6 and TIM7)	Partial compatibility
PWR	Yes	Yes+	Enhancements: – Flash off – Regulator in low power only in Stop mode	Identical for the same feature	Partial compatibility
RCC	Yes	Yes+	New features added: – HSI after stop mode – crystal-less USB – HSI48 added – LSE driving strength	Identical for the same feature	Partial compatibility
USART	Yes	Yes+	Choice for independent clock sources, time-out feature, wake-up from stop mode, auto-baud rate	Identical	Full compatibility
I2C	Yes	Yes++	Communication events managed by hardware, FM+, wake up from stop mode, digital filter, independent clock option	Identical	New driver
DAC	Yes	Yes	Same features, only one DAC	Identical	Full compatibility
ADC	Yes	Yes++	New analog part, new digital interface, oversampling feature, VLCD input, reduced analog inputs	Identical (for reduced analog inputs)	New driver
RTC	Yes	Yes+	Same features, tamper pins configuration extension	Identical	Full compatibility
FLASH	Yes	Yes	Option byte modified	NA	Partial compatibility
GPIO	Yes	Yes	Same features	Identical	Full compatibility
Firewall	NA	Yes	New peripheral	NA	New driver
USB FS Device	Yes	Yes+	Support low-power mode (LPM) and battery charging detection	Identical	Partial compatibility
CRS	NA	Yes	New peripheral	NA	NA

Table 4. STM32 peripheral compatibility analysis, STM32L1 vs. STM32L0 series(1) (continued)

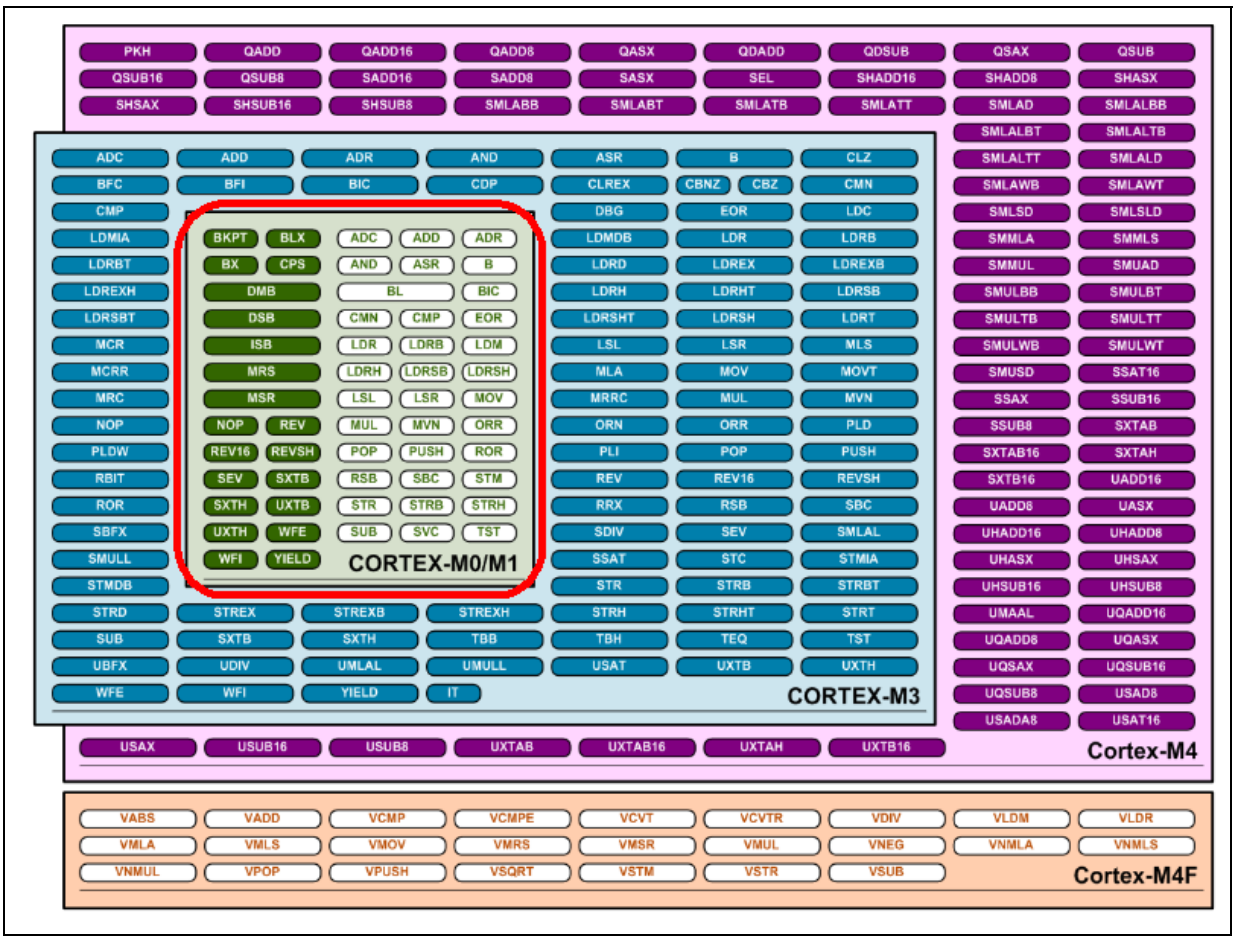
Peripheral	STM32L1	STM32L0	Compatibility		
			Features	Pinout	Firmware
Touch sensing	Yes	Yes++	New architecture: full hardware management	Partial	New driver
COMP	Yes	Yes+	New comparators design	Partial	New driver
SYSCFG	Yes	Yes+	New functionality added	NA	Partial compatibility
SDIO	Yes	NA	NA	NA	NA
FSMC	Yes	NA	NA	NA	NA
OPAMP	Yes	NA	NA	NA	NA
LCD	Yes	Yes+	Added SEG pins remap	Identical	Full compatibility
AES	Yes	Yes	Same features	NA	Full compatibility
RNG	NA	Yes	New peripheral	NA	New driver
LPUART	NA	Yes	New peripheral	NA	New driver
LPTIM	NA	Yes	New peripheral	NA	New driver

1. Yes++ = New feature or new architecture,
Yes+ = Same feature, but specification change or enhancement,
Yes = Feature available,
NA = Feature not available

3.2 System architecture

The STM32L0xx MCU family has been designed to target an entry-level market, with low-power capabilities and easy handling. In order to fulfill this aim while keeping the advanced high-end features proper to the STM32, the core has been changed for a ARM® Cortex®-M0+. Its small silicon area, coupled to a minimal code footprint, allows for low-cost applications with 32-bit performance. *Figure 1* shows the correspondence between the Cortex®-M4 and Cortex®-M0+ sets of instructions. Moving from STM32L1 to STM32L0 series requires a recompilation of the code to avoid the use of unavailable features.

Figure 1. System architecture



Important modifications have been performed on the MCU organization too, starting by switching from a Harvard to Von Neumann architecture, decreasing the system complexity, or focusing on SW Debug in order to simplify this precise feature.

3.3 Memory mapping

The peripheral address mapping has been changed in the STM32L0 series. The main change concerns the GPIOs which have been moved from the AHB bus to the IOPORT bus to allow them to operate at the maximum speed.

3.4 Reset and clock controller (RCC) interface

The main differences related to the RCC (Reset and clock controller) in the STM32L0 series versus STM32L1 series are presented in *Table 5*.

Table 5. RCC differences between STM32L1 and STM32L0 series

RCC	STM32L1 series	STM32L0 series
HSI 48	NA	High speed internal oscillator at 48MHz
HSI	8 MHz RC factory-trimmed	Similar, can be used after wake-up from the Stop mode
LSI	37 kHz RC	Similar
HSE	1 - 32 MHz	1 - 32 MHz(1)
LSE	32.768 kHz	32.768 kHz driving strength control
PLL	Main PLL	Similar
System clock source	HSI, HSE, MSI or PLL	Similar
System clock frequency	Up to 32 MHz MSI = 2.097 MHz after reset	Similar
APB1/APB frequency	Up to 32 MHz	Similar
RTC clock source	LSI, LSE or HSE	Similar
MCO clock source	SYSCLK, HSI, MSI, HSE, PLL, LSI, LSE	SYSCLK, HSI, MSI, HSE, PLL, LSI, LSE, HSI48
Internal oscillator measurement / calibration	LSI, MSI, HSI can be measured with respect to LSE or HSE clock by using TIM9, TIM10 or TIM11.	LSI, MSI, HSI can be measured with respect to LSE or HSE clock by using TIM21. HSI48 can be calibrated on the run by the mean of the CRS using a reference clock.

1. Same feature but spec change or enhancement

3.5 DMA interface

The STM32L1 and STM32L0 series use the same fully compatible DMA controller.

The STM32L0 series uses one 7-channel DMA controller, while the STM32L1 series uses one 7-channel DMA controller and an additional 5-channel DMA controller.

Each channel is dedicated to managing memory access requests from one or more peripherals.

The tables below present the correspondence between the DMA requests of the peripherals in STM32L1 series and STM32L0 series.

Table 6. DMA request differences between STM32L1 series and STM32L0 series

Peripheral	DMA request	STM32L1 series	STM32L0 series
ADC1 / ADC	ADC1 / ADC	DMA1_Channel1	DMA_Channel1 / DMA_Channel2
DAC	DAC DAC_Channel1 DAC_Channel2	DMA1_Channel2 (DAC_Channel1) DMA1_Channel3 (DAC_Channel2)	DMA_Channel3
SPI1	SPI1_Rx SPI1_Tx	DMA1_Channel2 DMA1_Channel3	DMA_Channel2 DMA_Channel3
SPI2	SPI2_Rx SPI2_Tx	DMA1_Channel4 DMA1_Channel5	DMA_Channel4 DMA_Channel5
USART1	USART1_Rx USART1_Tx	DMA1_Channel5 DMA1_Channel4	DMA_Channel3 / DMA_Channel5 DMA_Channel2 / DMA_Channel4
USART2	USART2_Rx USART2_Tx	DMA1_Channe6 DMA1_Channel7	DMA_Channel5 / DMA_Channel6 DMA_Channel4 / DMA_Channel7
I2C1	I2C1_Rx I2C1_Tx	DMA1_Channe7 DMA1_Channel6	DMA_Channel3 / DMA_Channel7 DMA_Channel2 / DMA_Channel6
I2C2	I2C2_Rx I2C2_Tx	DMA1_Channel5 DMA1_Channel4	DMA_Channel5 DMA_Channel4
TIM2	TIM2_UP TIM2_CH1 TIM2_CH2 TIM2_CH3 TIM2_CH4	DMA1_Channel2 DMA1_Channel5 DMA1_Channel7 DMA1_Channel1 DMA1_Channel7	DMA_Channel2 DMA_Channel5 DMA_Channel3 / DMA_Channel7 DMA_Channel1 DMA_Channel4 / DMA_Channel7
AES	AES_IN AES_OUT	DMA2_Channel5 DMA2_Channel3	DMA1_Channel5 / DMA1_Channel1 DMA1_Channel3 / DMA1_Channel2

3.6 Interrupt vectors

Table 7 presents the interrupt vectors of the STM32L0 series vs. the STM32L1 series (in this table, NA means that the feature is not available).

The switch from ARM® Cortex®-M4 to ARM® Cortex®-M0+ has requested a reduction of the vector table. This leads to several differences between the two devices.

Table 7. Interrupt vector difference

Position	STM32L1 series	STM32L0 series
0	WWDG	WWDG
1	PVD	PVD
2	TAMPER	RTC
3	RTC	FLASH
4	FLASH	RCC_CRS
5	RCC	EXTI[1:0]
6	EXTI0	EXTI[3:2]
7	EXTI1	EXTI[15:4]
8	EXTI2	TSC
9	EXTI3	DMA_CH1
10	EXTI4	DMA_CH[3:2]
11	DMA1_Channel1	DMA_CH[7:4]
12	DMA1_Channel2	ADC, COMP
13	DMA1_Channel3	LPTIM1
14	DMA1_Channel4	-
15	DMA1_Channel5	TIM2
16	DMA1_Channel6	-
17	DMA1_Channel7	TIM6, DAC
18	ADC1	-
19	USB_HP	-
20	USB_LP	TIM21
21	DAC	-
22	COMP, TSC	TIM22
23	EXTI9_5	I2C1
24	LCD	I2C2
25	TIM9	SPI1
26	TIM10	SPI2
27	TIM11	USART1
28	TIM2	USART2

Table 7. Interrupt vector difference (continued)

Position	STM32L1 series	STM32L0 series
29	TIM3	LPUART1, AES, RNG
30	TIM4	LCD
31	I2C1_EV	USB
32	I2C1_ER	NA
33	I2C2_EV	NA
34	I2C2_ER	NA
35	SPI1	NA
36	SPI2	NA
37	USART1	NA
38	USART2	NA
39	USART3	NA
40	EXTI15_10	NA
41	RTC_Alarm	NA
42	USB_FS_WKUP	NA
43	TIM6	NA
44	TIM7	NA
45	SDIO	NA
46	TIM5	NA
47	SPI3	NA
48	UART4	NA
49	UART5	NA
50	DMA2_CH1	NA
51	DMA2_CH2	NA
52	DMA2_CH3	NA
53	DMA2_CH4	NA
54	DMA2_CH5	NA
55	AES	NA
56	COMP_ACQ	NA

3.7 GPIO interface

The STM32L0 GPIO peripheral embeds new features compared to STM32L1 series:

- GPIO mapped on IOPORT bus for better performance
- More possibilities and features for I/O configuration.

Alternate function mode

Alternate function configuration is similar for both products, the STM32L0 series has reduced number of alternate functions in comparison to STM32L1 series. Consequently, different alternate function number on given pin should be used for the same alternate function.

Please refer to the “Alternate function mapping” table in the STM32L0 and STM32L1 datasheets for the detailed mapping of the system and the peripheral alternate function I/O pins.

3.8 EXTI source selection

In STM32L0 some of the EXTI lines are direct: they are used by some peripherals to generate a wakeup from Stop event or interrupt. In this case the status flag is provided by the peripheral.

Other changes are only in number of EXTI lines: on STM32L0 there are 30 lines (22 configurable, and 7 direct), on STM32L1 there are 24 lines.

3.9 Timers (TIM)

In STM32L0 there is a modified set of timers (TIM2, TIM3,TIM6, TIM7, TIM21 and TIM22) and a new one (LPTIM1) optimized for low power consumption and run in low power modes.

In STM32L1 the list of timers is made up of TIM2, TIM3, TIM4, TIM5, TIM6, TIM7, TIM9, TIM10 and TIM11.

Synchronization capabilities can differ between timers, the user has to check details in the already cited reference manuals. *Table 8* details the different configurations, the fully compatible timers are TIM2, TIM3, TIM6 and TIM7.

Table 8. Timers configuration for STM32L0 and STM32L1 series

Series	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
L0	TIM21 TIM22	16-bit	Up, down, up/down	Any integer between 1 and 65536	No	2	No
L1	TIM4	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
	TIM5	32-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
	TIM9	16-bit	Up, down, up/down	Any integer between 1 and 65536	No	2	No
	TIM10 TIM11	16-bit	Up	Any integer between 1 and 65536	No	1	No

Table 8. Timers configuration for STM32L0 and STM32L1 series (continued)

Series	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/compare channels	Complementary outputs
L0 and L1	TIM2 TIM3	16-bit	Up, down, up/down	Any integer between 1 and 65536	Yes	4	No
	TIM6 TIM7	16-bit	Up	Any integer between 1 and 65536	Yes	0	No

3.10 Flash interface

Table 9 presents the difference between the Flash interface of STM32L1 series and STM32L0 series (in this table, NA means that the feature is not available).

Table 9. Flash differences between STM32L1 series and STM32L0 series(1)

FLASH		STM32L1 series	STM32L0 series
Main/Program memory	Start Address	0x0800 0000	0x0800 0000
	End Address	Up to 0x0807 FFFF	Up to 0x0802 FFFF
	Granularity	Page of 256 bytes size	Page of 128 bytes size
EEPROM memory	Start Address	0x0808 0000	0x0808 0000
	End Address	Up to 0x0808 3FFF	Up to 0x0808 17FF
System memory	Start Address	0x1FF0 0000	0x1FF0 0000
	End Address	0x1FF0 0FFF	0x1FF0 0FFF
Option Bytes	Start Address	0x1FF8 0000	0x1FF8 0000
	End Address	0x1FF8 00FF	0x1FF8 007F
Read Protection	Unprotection	Level 0 no protection RDP = 0xAA	Level 0 no protection RDP = 0xAA
	Protection	Level 1 memory protection RDP ! = (Level 2 & Level 0) Level 2 memory protection RDP = 0xCC(3)	Level 1 memory protection RDP != (Level 2 & Level 0) Level 2: Lvl 1 +Debug disabled RDP = 0xCC PCROP protection
Write protection		Protection by 4 Kbytes	Protection by 4 Kbytes

Table 9. Flash differences between STM32L1 series and STM32L0 series(1) (continued)

FLASH	STM32L1 series	STM32L0 series
User Option bytes	BOR_LEV[3:0]	BOR_LEV[3:0]
	WDG_SW	WDG_SW
	nRTS_STOP	nRTS_STOP
	nRST_STDBY	nRST_STDBY
	BFB2	BFB2
	NA	IWDG_ULP
	NA	BOOT_SEL
	NA	nBOOT0
	nBOOT1	nBOOT1
Erase granularity	Page	Page
Program mode	Word / Half page	Word / Half page

1. NA in gray table cells means Not Applicable.

3.11 ADC interface

The table below presents the differences between the ADC interface of STM32L1 series and STM32L0 series; these differences are the following:

- New analog design
- New digital interface
- New architecture and new features

Table 10. ADC differences between STM32L1 series and STM32L0 series

ADC	STM32L1 series		STM32L0 series
Type	SAR structure		SAR structure
Repartition	ADC1, ADC2		ADC
Max sampling freq	1 MSPS		1.14 MSPS
Number of channels	Up to 40 channels + 2 internal		Up to 16 channels + 3 internal(1)
Resolution	12-bit		12-bit (16-bit with hardware oversampling)
Conversion Modes	Single / Continuous / Scan / Discontinuous / Dual Mode		Single / Continuous / Scan / Discontinuous
DMA	Yes		Yes
External Trigger	External event for regular channels: – TIM9_CC2 – TIM9_TRGO – TIM2_CC3 – TIM2_CC2 – TIM3_TRGO – TIM4_CC4 – TIM2_TRGO – TIM3_CC1 – TIM3_CC3 – TIM4_TRGO – TIM6_TRGO – EXTI line11	External event for injected channels: – TIM9_CC1 – TIM9_TRGO – TIM2_TRGO – TIM2_CC1 – TIM3_CC4 – TIM4_TRGO – TIM4_CC1 – TIM4_CC2 – TIM4_CC3 – TIM10_CC1 – TIM7_TRGO – EXTI line15	TIM6_TRGO TIM21_CH2 TIM2_TRGO TIM2_CH4 TIM22_TRGO TIM2_CH3 TIM3_TRGO EXTI line 11
Supply requirement	1.8 to 3.6 V		1.65 to 3.6 V
Input range	Vref- ≤ Vin ≤ Vref+		$V_{SSA} \leq V_{IN} \leq V_{DDA} \leq 3.6$ V

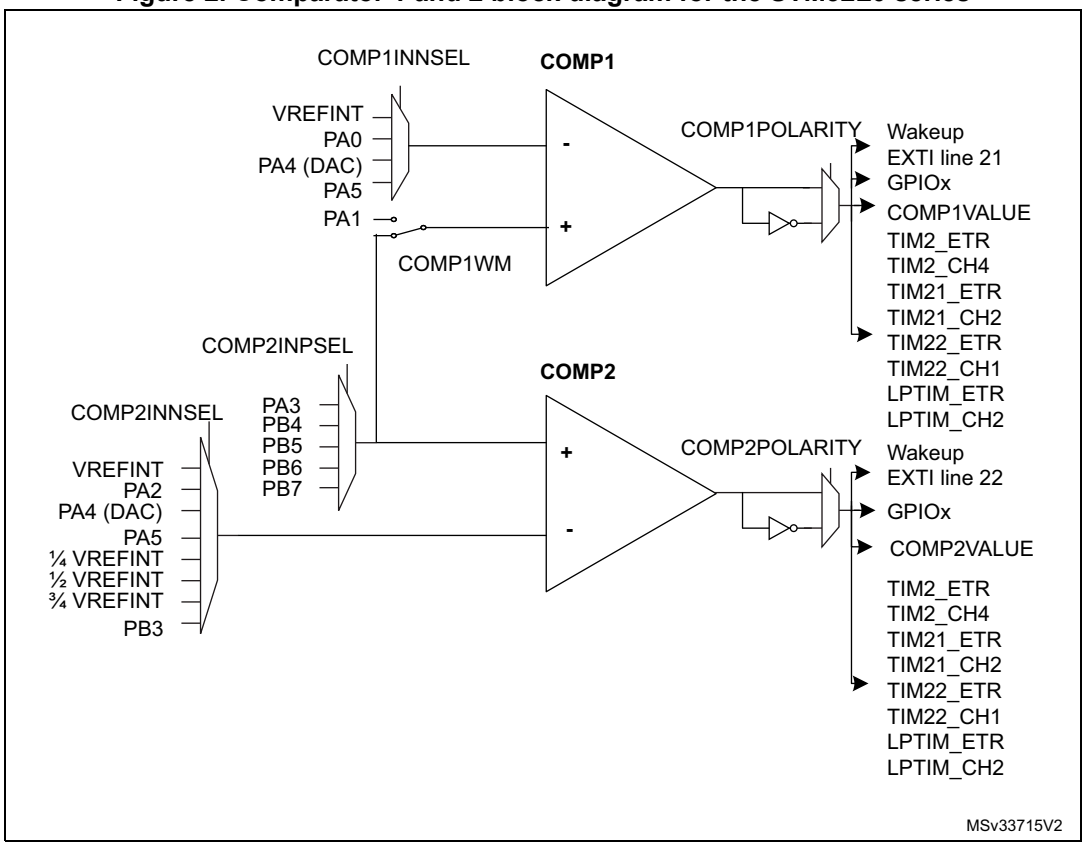
1. Same feature but specification change or enhancement.

3.12 COMP interface

The STM32L0 series embeds the same comparators COMP1 (ultra low consumption) and COMP2 (rail-to-rail) used by the STM32L1 series, but are there different input and output connections.

Figure 2 illustrates the block diagram for comparators of the STM32L0 series.

Figure 2. Comparator 1 and 2 block diagram for the STM32L0 series



Microcontrollers of the STM32L1 series use different comparators interconnections. The block diagrams for different STM32L1 categories are shown in figures *3*, *4*, *5* and *6*.

Figure 3. COMP1 interconnections (Cat.1 and Cat.2 devices), STM32L1 series

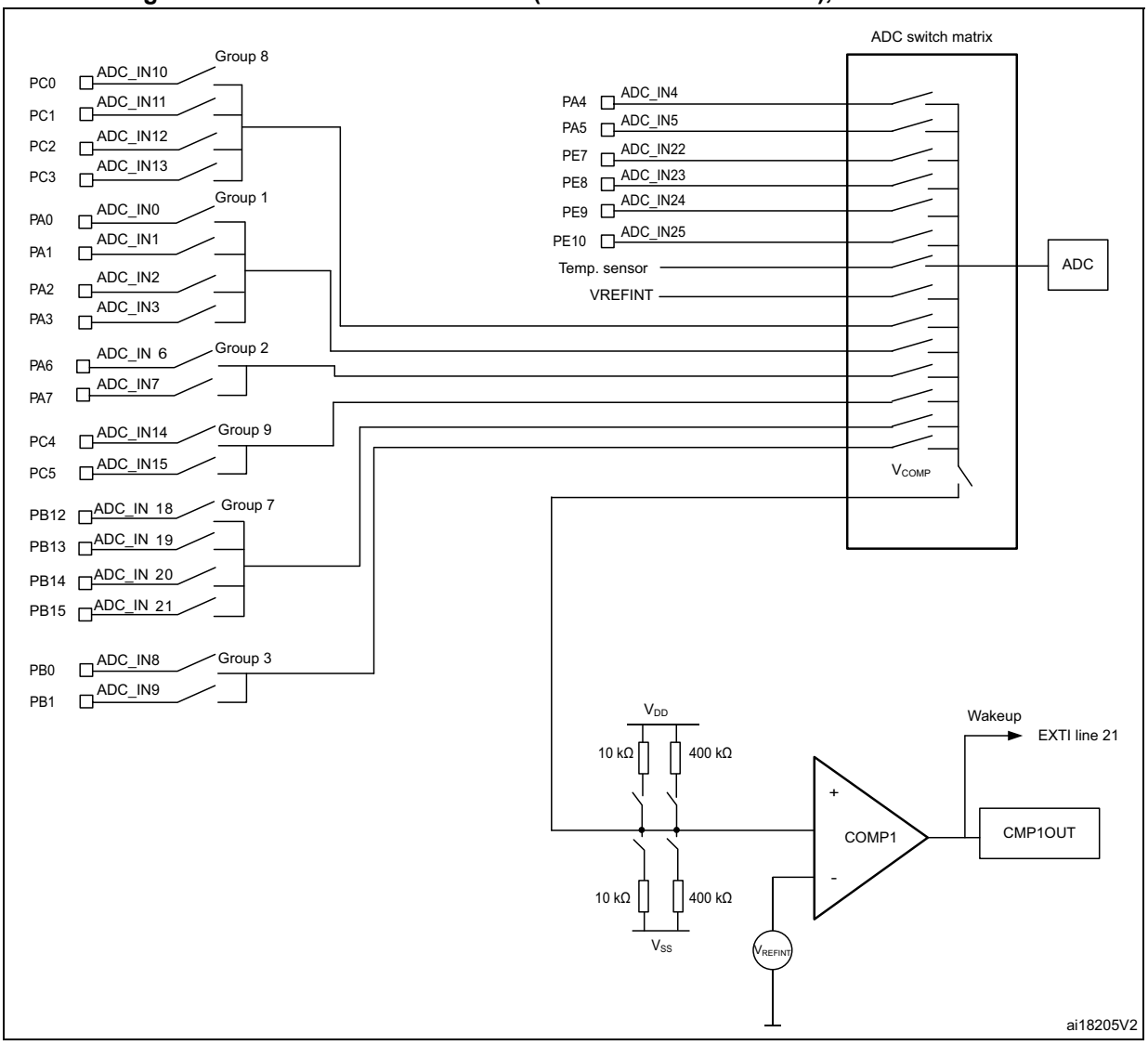


Figure 4. COMP1 interconnections (Cat.3, Cat.4, Cat.5 and Cat.6 devices), STM32L1 series

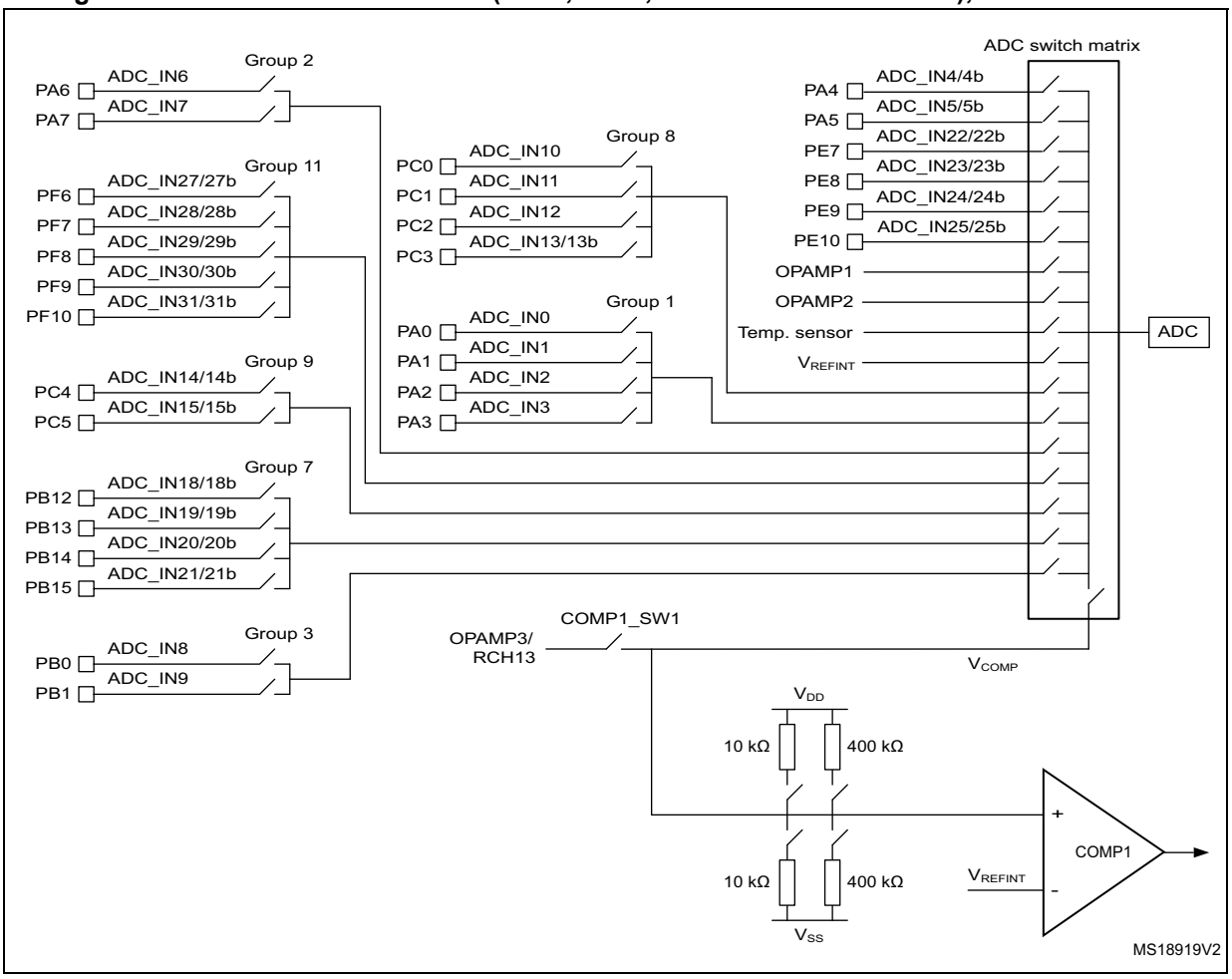


Figure 5. COMP2 interconnections (Cat.1 and Cat.2 devices), STM32L1 series

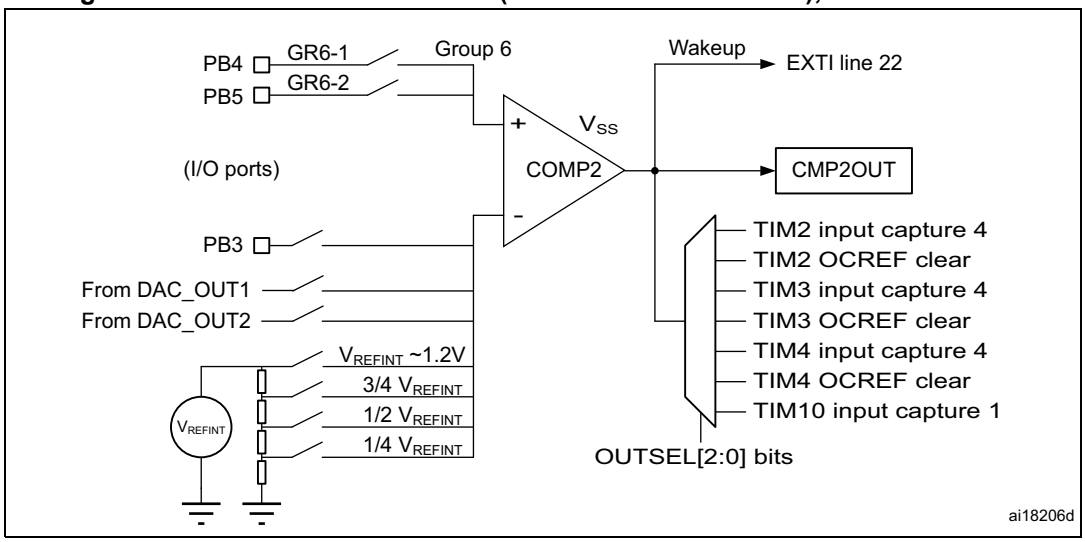
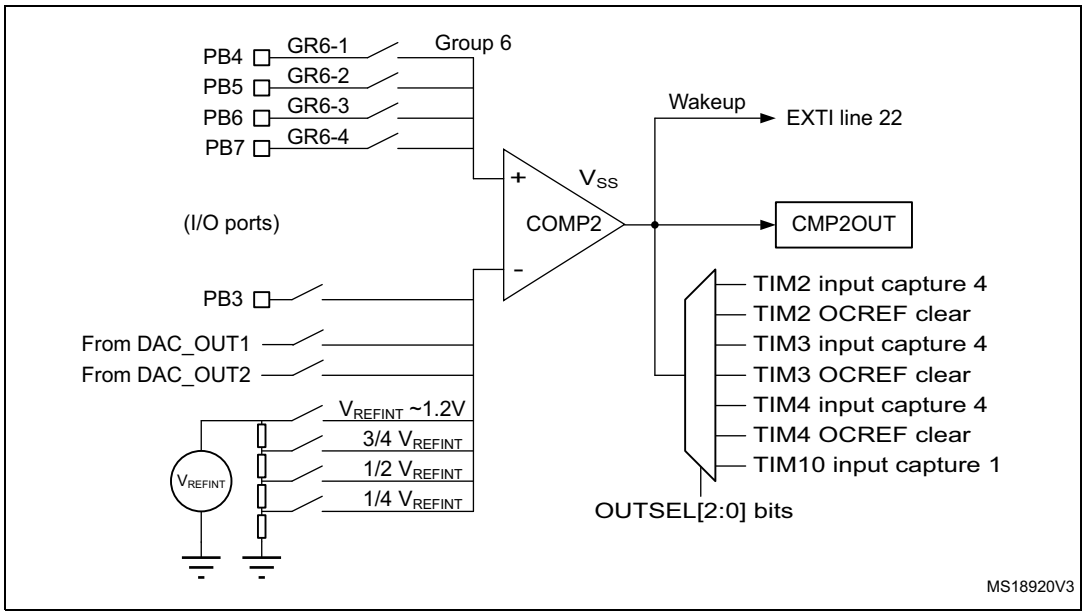


Figure 6. COMP2 interconnections (Cat.3, Cat.4, Cat.5 and Cat.6 devices), STM32L1 series



3.13 PWR interface

In STM32L0 series the PWR controller presents some differences vs. STM32L1 series, these differences are summarized in *Table 11*. The programming interface is unchanged.

Table 11. PWR differences between STM32L1 series and STM32L0 series

PWR	STM32L1 series	STM32L0 series
Power supplies	1-VDD = 1.8 V (at power on) or 1.65 V (at power down) to 3.6 V when the BOR is available and VDD = 1.65 to 3.6 V, when BOR is not available. 2-VDDA = 1.8 V (at power on) or 1.65 V (at power down) to 3.6 V, when BOR is available and VDDA = 1.65 to 3.6 V, when BOR is not available. 3-VREF+ is the input reference voltage. It is only available as an external pin on a few packages, otherwise it's bonded to VDDA. 4-VLCD = 2.5 to 3.6 V	1-VDD = 1.8 V (at power on) or 1.65 V (at power down) to 3.6 V when the BOR is available and VDD = 1.65 to 3.6 V, when BOR is not available. 2-VDDA = 1.8 V (at power on) or 1.65 V (at power down) to 3.6 V, when BOR is available and VDDA = 1.65 to 3.6 V, when BOR is not available. 3-VREF+ is the input reference voltage. It is only available as an external pin on a few packages, otherwise it is bonded to VDDA. 4-VLCD = 2.5 to 3.6 V 5- VDD_USB = 3.0 to 3.6. VV DD_USB is a dedicated independent USB power supply for full speed transceivers.
Power supply supervisor	Integrated POR / PDR circuitry Programmable Voltage Detector (PVD) Brown-out reset (BOR)	Integrated POR / PDR circuitry Programmable Voltage Detector (PVD) / Brown-out reset (BOR)
Low-power modes	Low power run mode Sleep mode Low power sleep mode Stop mode Standby mode	Low power run mode Sleep mode Low power sleep mode Stop mode Standby mode
Wake-up sources	Sleep mode – Any peripheral interrupt/wakeup event Stop mode – Any EXTI (PVD, RTC, COMP, USB) line event/interrupt Standby mode – WKUP pin rising edge – RTC alarm – External reset in NRST pin – IWDG reset	Sleep mode – Any peripheral interrupt/wakeup event Stop mode – Any EXTI (PVD, RTC, COMP, USB, I2C, USART, LPUART, LPTIM)line event/interrupt Standby mode – WKUPx pins rising edge – RTC alarm / autowakeup – External reset in NRST pin – IWDG reset

3.14 Real-time clock (RTC) interface

The RTC interface in STM32L0 series is backward compatible with STM32L1 version. STM32L0 series implements enhancement in tamper inputs - possbility to not erase backup registers for given RTC_TAMPx input. In STM32L0 series was changed also RTC_ALARM_TYPE bit position for alarm output type selection.

3.15 SPI interface

The SPI interface was not changed in STM32L0 series and it's fully compatible with the STM32L1 version.

3.16 I2C interface

The STM32L0 series embeds a new I2C peripheral versus the STM32L1 series. The architecture, features and programming interface are different.

As a consequence, the STM32L0 I2C programming procedures and registers are different from those of the STM32L1 series, so any code written for the STM32L1 series using the I2C needs to be rewritten to run on STM32L0 series.

The STM32L0 I2C provides best-in-class new features:

- Communication events managed by hardware.
- Programmable analog and digital noise filters.
- Independent clock source: PCLK1, HSI or SYSCLK.
- Wake-up from STOP mode.
- Fast mode + (up to 1MHz) with 20mA I/O output current drive.
- 7-bit and 10-bit addressing mode, multiple 7-bit slave address support with configurable masks.
- Address sequence automatic sending (both 7-bit and 10-bit) in master mode.
- Automatic end of communication management in master mode.
- Programmable Hold and Setup times.
- Command and Data Acknowledge control.

For more information about STM32L0 I2C features, please refer to I2C section of STM32L0xx Reference Manual (RM0367).

3.17 USART interface

The STM32L0 series embeds a new USART peripheral versus the STM32L1 series. The architecture, features and programming interface are modified to introduce new capabilities.

As a consequence, the STM32L0 USART programming procedures and registers are modified from those of the STM32L1 series, so any code written for the STM32L1 series using the USART needs to be updated to run on STM32L0 series.

The STM32L0 USART provides best-in-class added features:

- A choice of independent clock sources allowing
  - UART functionality and wake-up from low power modes,
  - convenient baud-rate programming independently of the APB clock reprogramming.
- Smartcard emulation capability: T=0 with auto retry and T=1
- Swappable Tx/Rx pin configuration
- Binary data inversion
- Tx/Rx pin active level inversion
- Transmit/receive enable acknowledge flags
- New Interrupt sources with flags:
  - Address/character match
  - Block length detection and timeout detection
- Timeout feature
- Modbus communication
- Overrun flag disable
- DMA disable on reception error
- Wake-up from STOP mode
- Auto baud rate detection capability
- Driver Enable signal (DE) for RS485 mode

For more information about STM32L0 USART features, please refer to USART section of STM32L0xx Reference Manual (RM0367).

3.18 USB interface

The STM32L0 series embeds an enhanced USB peripheral versus the STM32L1 series. New features are introduced to provide more capabilities to users.

The STM32L0 USB provides best-in-class added features:

- Up to 1024 Bytes of dedicated packet buffer memory SRAM
- Battery Charging Specification Revision 1.2 support
- USB 2.0 Link Power Management (LPM) support
- Crystal-less capability with the HSI48 RC oscillator and the CRS, that can use the USB SOF signal to adjust the frequency on-fly

3.19 LCD interface

The STM32L0 series embeds the same LCD peripheral like in the STM32L1 series but there was extended number of segments. The LCD embedded in STM32L0 supports up to 8 common terminals and up to 52 segment terminals to drive 208 (4x52) or 384 (8x48) LCD picture elements (pixels).

The LCD embedded in STM32L1 supports up to 8 common terminals and up to 44 segment terminals to drive 176 (44x4) or 320 (40x8) LCD picture elements (pixels).

3.20 TSC interface

The STM32L0 series embeds enhanced version of touch sensing controller with full hardware support. Therefore the firmware must be rewritten to support those new architecture. The pinout compatibility for touch sensing channels was also partially changed and there is need to change/review the application hardware design.

3.21 AES interface

The AES interface has not been changed in STM32L0 series, consequently it's fully compatible with STM32L1 version.

4 Firmware migration using the library

For migration from existing STM32L1 firmware into new STM32L0 firmware is required that existing firmware was written using STM32 Cube. Then the migration should be very easy due to STM32 Cube compatibility for the same or similar peripherals features. For enhanced/different peripheral design is there needed to use modified functions for given peripheral.

5 Revision history

Table 12. Document revision history

Date	Revision	Changes
29-Apr-2015	1	Initial release.