
The STUSB4761 PCB routing guidelines

Introduction

This document provides some information about how to route the STUSB4761 PCB while the STUSB4761 USB power delivery controller is being implemented.

The STUSB4761 is a USB power delivery controller, which natively embeds current control and voltage control (CC/CV features).

In order to sense properly both the current and voltage, basic routing rules need to be followed while PCB is being designed.

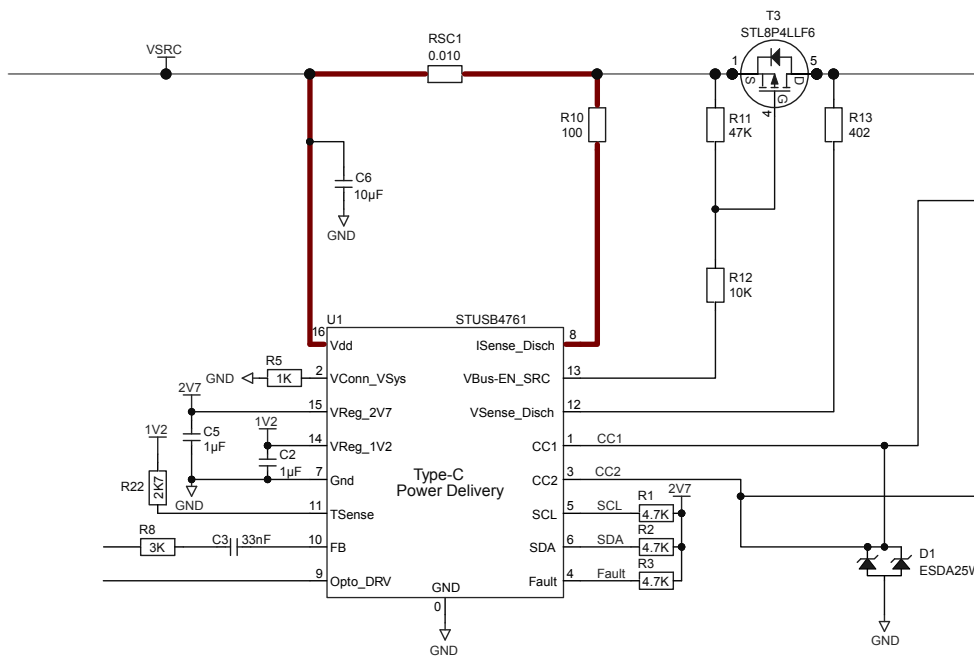
1 Current sensing

The STUSB4761 embeds a current sensing feature, which is used to limit the current to output, if sink draws more than the STUSB4761 source capability.

When the current drawn by sink exceeds the STUSB4761 current settings, the STUSB4761 first goes to CC mode before triggering an overcurrent protection.

1.1 Current sensing path location

Figure 1. Current sensing path



Pins VDD and ISENSE_DISCH are used to monitor the current flowing into external current sensing resistor RSC1.

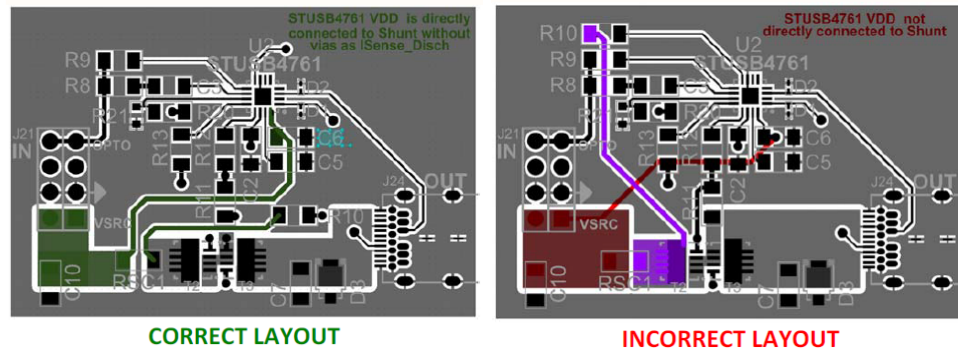
As current monitoring is done through the voltage comparison, it is important that:

- VDD and ISENSE_DISCH are connected in the same manner to guarantee the symmetry
- RSC1 is connected directly to VDD and ISENSE_DISCH through a dedicated path, in order to avoid voltage drops, which can impact the measurement

1.2 Current path PCB routing

VDD needs to be connected to Rshunt resistor, avoiding the current in the sensing path.
See the routing example below:

Figure 2. Good versus wrong layout



On the left side, VDD is directly connected to the shunt resistor without vias. ISENSE_DISCH is also directly connected to the other side of the shunt resistor, without vias. The two paths do not cross each other.

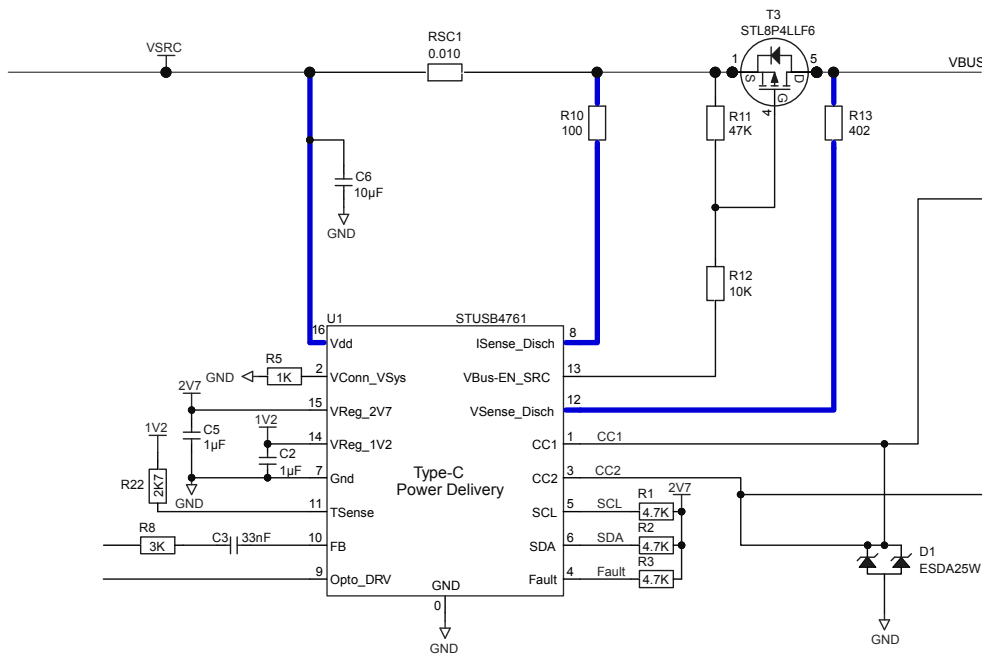
On the right side, VDD is not directly connected to shunt resistor but has some vias to change the layer level. The paths must not be crossed in order to avoid the cross coupling. Paths are not directly connected on the resistor path, which introduced a parasitic resistor.

2 Voltage sensing and discharge

In order to guarantee a ramp-down transition and safety at the connector level, the STUSB4761 monitors voltages on both sides of power switch paths.

2.1 Voltage sensing path location

Figure 3. Voltage monitoring and discharge paths



VDD input pin is used either for current sensing, or to check that VSRC is in the expected range. At the connection, it guarantees that power path is not closed if V_{dd} is out of V_{safe} 5 V range.

ISENSE_DISCH pin is used either for current sensing, or as VSRC discharge path during the voltage down transition, since the current sensing is not needed during this phase. This path helps to speed up VSRC input voltage discharge. Resistor needs to be selected in order to guarantee less than 500 mA as input current in ISENSE_DISCH pin.

VSENSE_DISCH pin is used to either monitor VBUS voltage at connector side, or to discharge VBUS on cable side during voltage down transition. Resistor needs to be selected in order to guarantee less than 50 mA input current in VSENSE_DISCH pin.

2.2 Voltage discharge path PCB recommendations

USB power delivery standard has a maximum time for VBUS transition defined at 275 ms.

Power path is opened when VBUS is below V_{safe5V} . The worst case transition for voltage on ISENSE_DISCH is then from maximum PDO voltage (20 V at maximum) down to V_{safe5V} (4.75 V to 5.5 V as per standard).

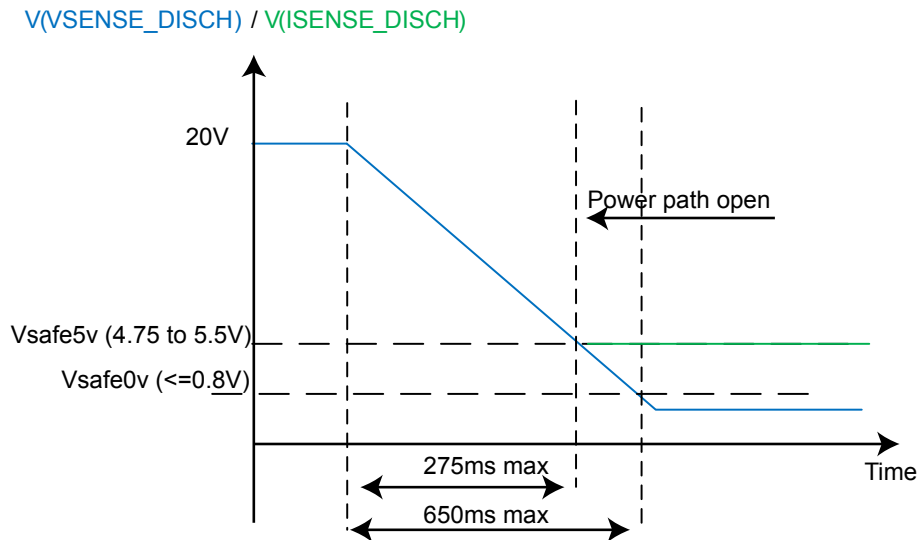
The worst case transition for voltage on VSENSE_DISCH is from maximum PDO voltage (20 V at maximum) down to V_{safe0V} (below 0.8 V). Consequently, discharge resistors need to be selected by taking into account the worst case of power dissipation versus max. allowed current.

Table 1. Current and timing constraints

STUSB4761 pin	Maximum current allowed on the STUSB4761 pin	Max. voltage gap to be discharged	Maximum time allowed for transition
ISENSE_DISCH	500 mA	15 V (20 V down to V_{safe5v})	275 ms
VSENSE_DISCH	50 mA	20 V (20 V down to V_{safe0v})	275 ms for 15 V voltage gap 375 ms for discharging V_{safe5v} to V_{safe0v}

Power dissipation of the resistor must be taken into account during the selection.

Figure 4. Timing constraints



Revision history

Table 2. Document revision history

Date	Version	Changes
16-Dec-2019	1	Initial release.

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