Ultra-low-power features of STM32WL Series microcontrollers

Introduction

The STM32WL Series microcontrollers are long-range wireless and ultra-low-power devices (named STM32WL devices in this document) and embed a powerful and ultra-low-power LPWAN-compliant radio solution. These devices are designed to be extremely low-power and are based on the high-performance Arm® Cortex®-M4 32-bit RISC core that operates at a frequency of up to 48 MHz. It is complemented by an Arm® Cortex®-M0+.

The STM32WL devices feature a flexible management of the power modes, allowing the overall application consumption to be reduced.

A large number of smart and high-performance peripherals, a large set of advanced and low-power analog features, and several peripherals tuned for low-power modes are embedded. By using the batch acquisition mode (BAM), these peripherals optimize the power consumption when data is transferred using the communication peripherals, while the rest of the device is kept in low-power mode.

The STM32WL devices enable an easy migration from a dual-chip solution (such as STM32L4 Series MCU + LoRa® / sub-GHz module), to a single chip, with a better power budget.

An embedded SMPS improves the power consumption in the applications, as well as the overall consumption for the sub-GHz radio communications.

Thanks to the built-in internal voltage regulator and voltage scaling, the device consumption in active modes is kept at a minimum, whatever the external supply voltage. This makes the STM32WL devices particularly suited for hand-held battery-powered products, down to 1.8 V. In addition, multi-voltage domains supply the devices at low voltage (further reducing consumption), while the analog-to-digital converters operate with a higher supply and reference voltage, up to 3.6 V.

The STM32WL devices support a battery Backup domain to keep the RTC running, and a set of 20 registers (32-bit wide), that can be retained in case of power loss. This optional backup battery can be charged when the main supply is present.

The various supported low-power modes allow the user to achieve the best compromise between low-power consumption, shorter start-up time, available set of peripherals and maximum number of wakeup sources.

1 Energy-efficient processing

The high-processing performance in Run mode (in DMIPS/MHz) is achieved thanks to the Arm® Cortex®-M4 core and its associated memory interfaces used in the STM32WL devices.

Note: Arm is a registered trademark of Arm Limited (or its subsidiaries) in the US and/or elsewhere.

The embedded ART Accelerator ensures full operating performance up to 48 MHz, by masking the Flash memory access wait-state. 1.25 DMIPS/MHz can be achieved, whatever the system clock frequency.

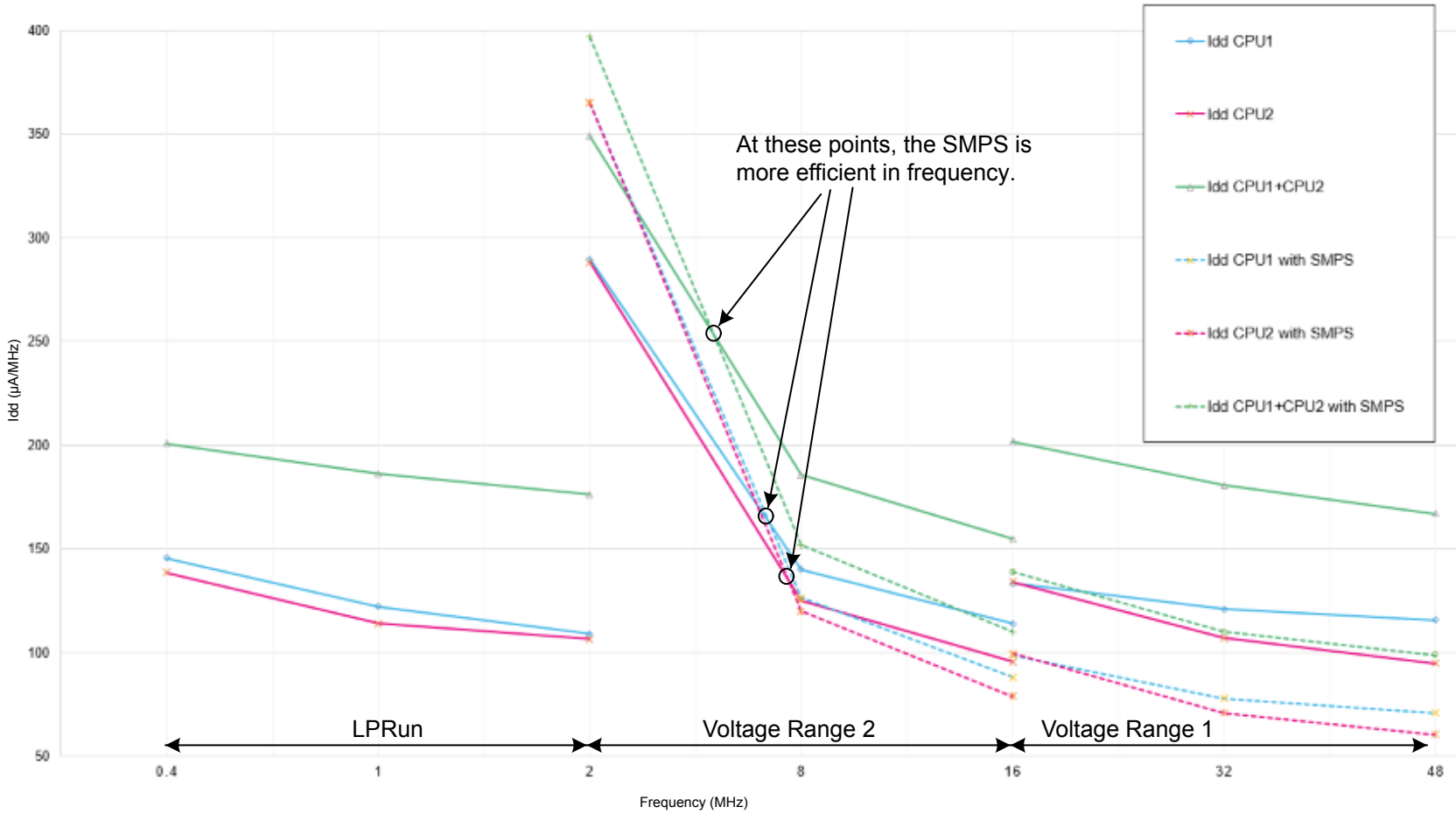
The "undervolting" method (adapt dynamically the internal supply voltage to the operating frequency) is used to reach a high-energy efficiency (in mA/DMIPS). STM32WL devices offer the following dynamically selectable voltage and frequency ranges:

- Range 1 for a system frequency up to 48 MHz
- Range 2 for a system frequency up to 16 MHz, with improved efficiency by 20% at 16 MHz versus Range 1

Thanks to the dedicated LPRun (low-power run) mode, the core can operate at 2 MHz and lower, with improved efficiency by 60% at 2 MHz versus Range 2, mainly due to the sub-GHz radio going into Deep-Sleep in LPRun mode.

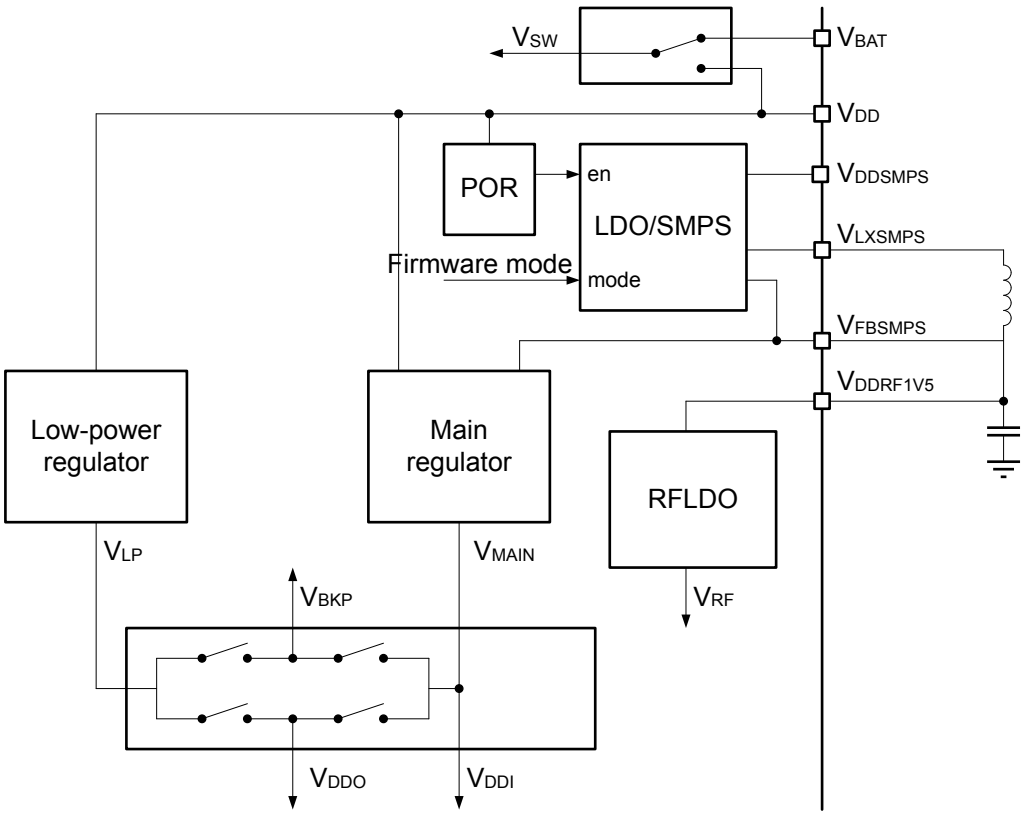
Figure 1 shows the typical current consumption of the STM32WL devices, from LDO and SMPS, versus system frequency and power modes (reminder: CPU1 = Cortex-M4 and CPU2 = Cortex-M0+, only available on the STM32WL5x devices).

Figure 1. Current consumption in Run mode versus frequency (3V, 25 °C)



The figure below shows the power distribution from the internal LDO regulators in the different Run modes.

Figure 2. Power supply overview



The STM32WL devices allow the Cortex-M4 (CPU1) to execute code either from the Flash memory, or from SRAM1 or SRAM2.

The lowest power consumption is achieved by running from an internal SRAM. When running from the internal Flash memory, the ART Accelerator reduces the number of memory accesses, thus reducing the overall current consumption.

The location of the executable code and data within the memory system, impacts not only the current consumption, but also the overall computation performance. As an example, the table below details the overall performances measured on a STM32WL55 device, with the system clock running at 48 MHz, executing a complex algorithm (such as CoreMark® from EEMBC® organization).

Table 1. STM32WL55 performance without SMPS, @ 48MHz

Configuration	mA/MHz	CoreMark per MHz	CoreMark per mA
Running from the Flash memory (cache on, prefetch buffer off)	0.116	3.40	29
Running from SRAM1 (code and data in SRAM1)	0.117	2.52	21

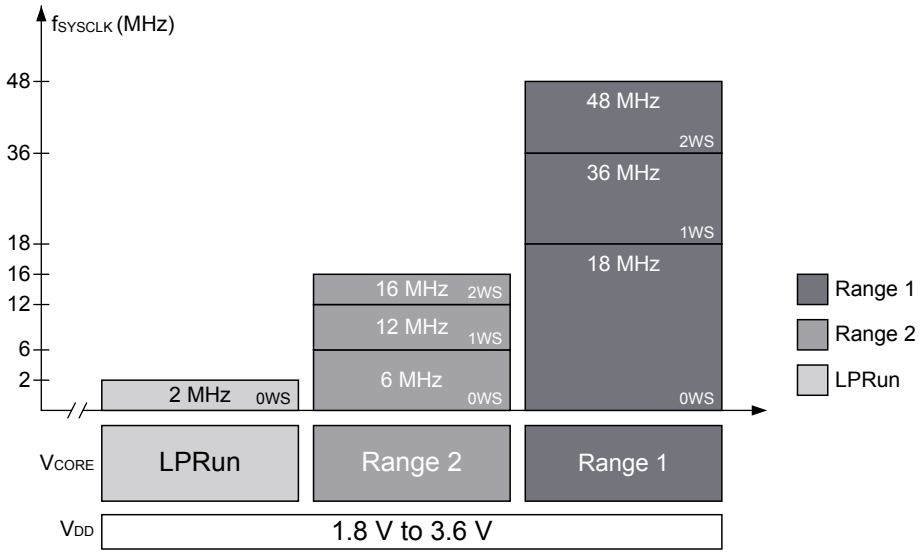
The ART Accelerator allows the Cortex-M4 core to run almost at the maximum efficiency. The table below shows that the SMPS improves the efficiency by ~34% (CoreMark per mA).

Table 2. STM32WL55 performance with SMPS, @ 48MHz

Configuration	mA/MHz	CoreMark per MHz	CoreMark per mA
Running from the Flash memory (cache on, prefetch buffer off)	0.071	3.40	48
Running from SRAM1 (code and data in SRAM1)	0.072	2.52	34

The figure below shows the STM32WL Flash memory latency (number of wait states to be programmed in the Flash memory access control register), versus the regulator voltage scaling range and the system clock frequency.

Figure 3. STM32WL Flash memory latency



2 Power modes

The application power consumption is reduced thanks to the power management flexibility, smart peripherals and the architecture.

The STM32WL devices feature an independent power management state between the sub-GHz radio and the CPUs. A dedicated hardware mechanism selects the lowest possible power consumption.

2.1 Low-power modes

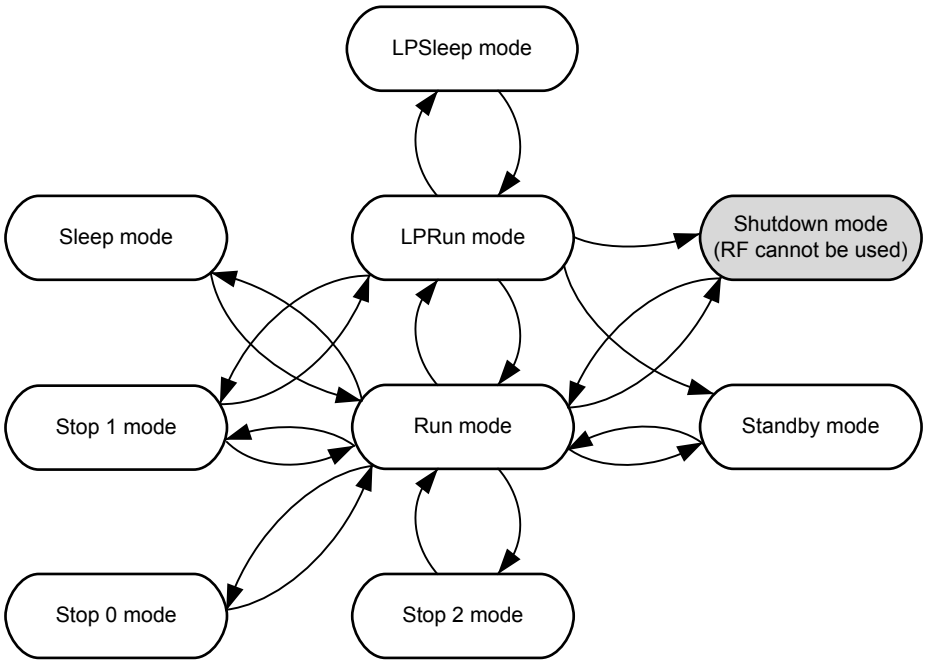
The STM32WL devices implement various low-power modes: Sleep, LPSleep, Stop 0/1/2, LPRun, Standby, Shutdown.

The power consumption can also be modulated by selecting different clock sources and frequencies, as well as clocking off unused peripherals.

In all these modes, except Shutdown, the power monitoring Brownout reset (BOR) and the IWDG (independent watchdog) can stay active to guarantee a safe execution.

The following sections outline the features available for each mode (refer to the product datasheet for more details). The figure below shows the possible transitions between the low-power modes.

Figure 4. Transitions between STM32WL low-power modes



2.1.1 Sleep mode

The Sleep mode is the low-power mode with the highest consumption, but with the benefit of the lowest wakeup latency and the SMPS use (if enabled).

In this mode, a further reduction of the consumption can be obtained by reducing the system clock frequency (compatible with peripherals remaining in Run mode).

2.1.2 LPRun and LPSleep modes

When the CPUs run below 2 MHz, the LPRun and LPSleep modes result in the best power performance. LPRun and LPSleep offer respectively Run and Sleep mode functionality for the user application, with extremely low current consumption, where some peripherals cannot be switched off, or where the CPU continuously processes at low speed to minimize current variations.

The following features are implemented to reduce the current consumption:

- The core logic is supplied by the low-power voltage regulator to reduce the quiescent current.
- The Flash memory can be switched off (power-down mode and clock gating) in LPSleep mode. The Flash memory can also be switched off in LPRun mode when the application processor executes from SRAM1.
- The system clock is limited to 2 MHz. The MSI internal RC oscillator can be selected as it supports several frequency ranges, with a small device total consumption (such as 48 µA in LPSleep, Flash memory off, at 100 kHz).

Batch acquisition mode (BAM)

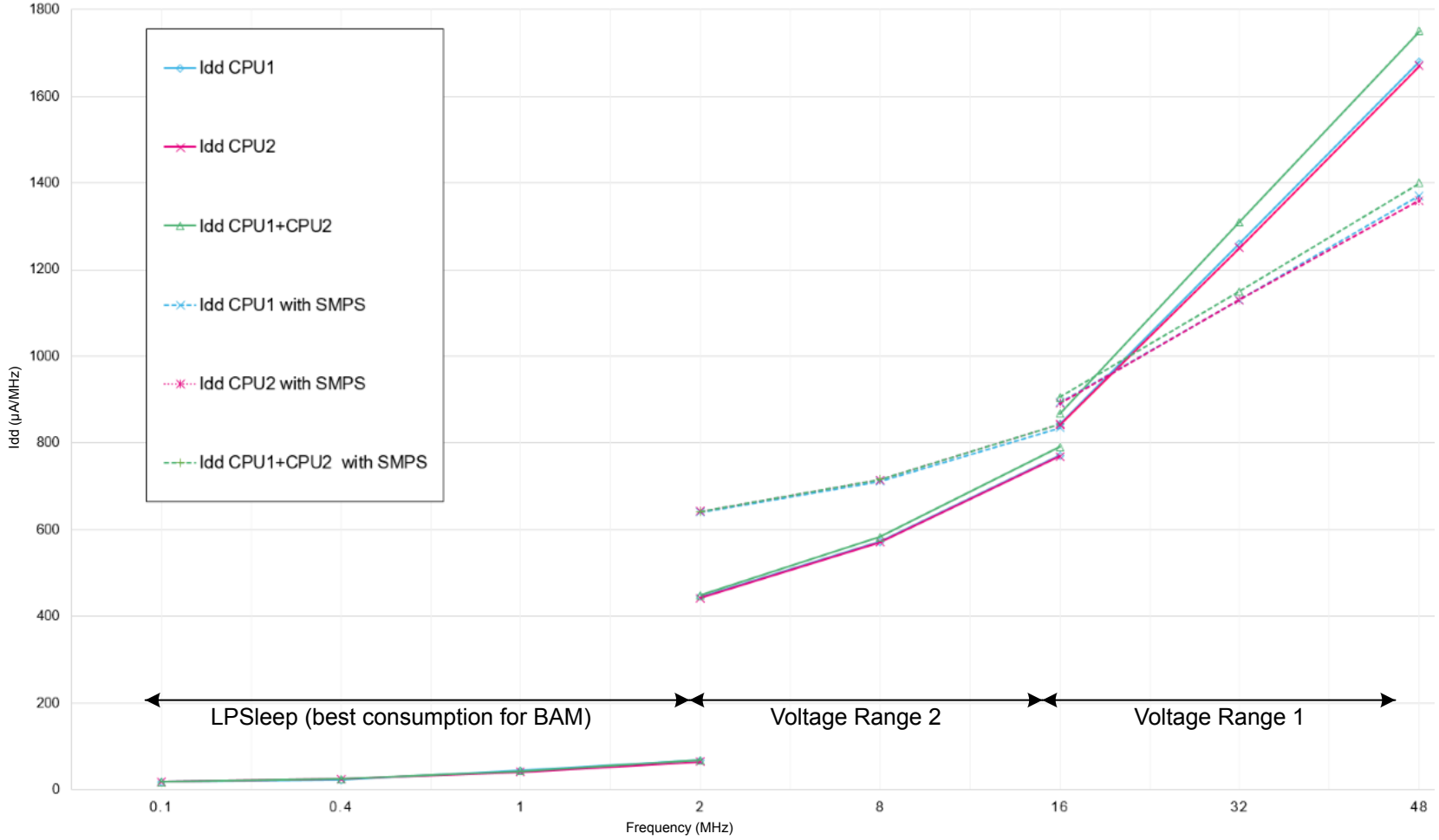
The STM32WL devices support the power efficient BAM, in which data is transferred using communication peripherals, while the device in Sleep or LPSleep mode, with the following configuration:

- Only the DMA, communication peripherals, and SRAM1 or SRAM2 clocks are enabled in Sleep (or LPSleep) mode.
- If the sub-GHz radio is not in use, the system clock can be limited to 2 MHz, and the main regulator is switched off (to enter LPSleep). In this case, the Flash memory can be powered off.

In LPSleep mode, the I2C and USART/LPUART peripherals can still be clocked with HSI at 16 MHz: BAM with I2C or USART can be supported at speeds up to 1 Mbit/s.

Important:
The user must change both frequency and voltage regulator to select the lowest power consumption, taking into account the wakeup-time and peripherals functionality at low frequency.

Figure 5. Current consumption in Sleep and LPSleep modes versus frequency (3V, 25 °C)



2.1.3 Stop modes

The STM32WL devices implement three Stop modes (Stop 0 , Stop 1, Stop 2), with full SRAM and peripheral retention, and a wakeup capabilities. In these Stop modes, all the high-speed oscillators (HSE, MSI, HSI) are stopped, while the active low-speed oscillators (LSE and/or LSI) are kept active. The peripherals are set to active using the HSI clock when needed, to wake up the device on a specific event (such as UART character reception or I2C address recognition).

2.1.4 Standby mode

In Standby mode, the BOR is always enabled, ensuring that the STM32WL device is reset if the supply voltage drops below the selected functional threshold. Individual pull-ups and pull-downs can be applied on each I/O during the Standby mode, preserving any external device configuration.

Wakeup from this mode is done by using one of the three wakeup pins, the reset pin or the IDWG. The RTC, clocked by a low-speed oscillator (LSE or LSI), is also functional in this mode, with wakeup capability.

Wakeup from this mode can also be performed by the sub-GHz radio.

2.1.5 Shutdown mode

The Shutdown mode is implemented in the STM32WL devices to further lengthen the battery autonomy of battery-powered applications. This mode provides the lowest power consumption, by switching off the internal voltage regulators and by disabling the voltage power monitoring.

Wakeup from this mode is done with one of the wakeup pins or the reset pin. The RTC, clocked by the LSE, is also functional in this mode, with wakeup capability. Wakeup from shutdown is equivalent to a POR (power-on reset).

Note: In this mode, the sub-GHz radio cannot be used.

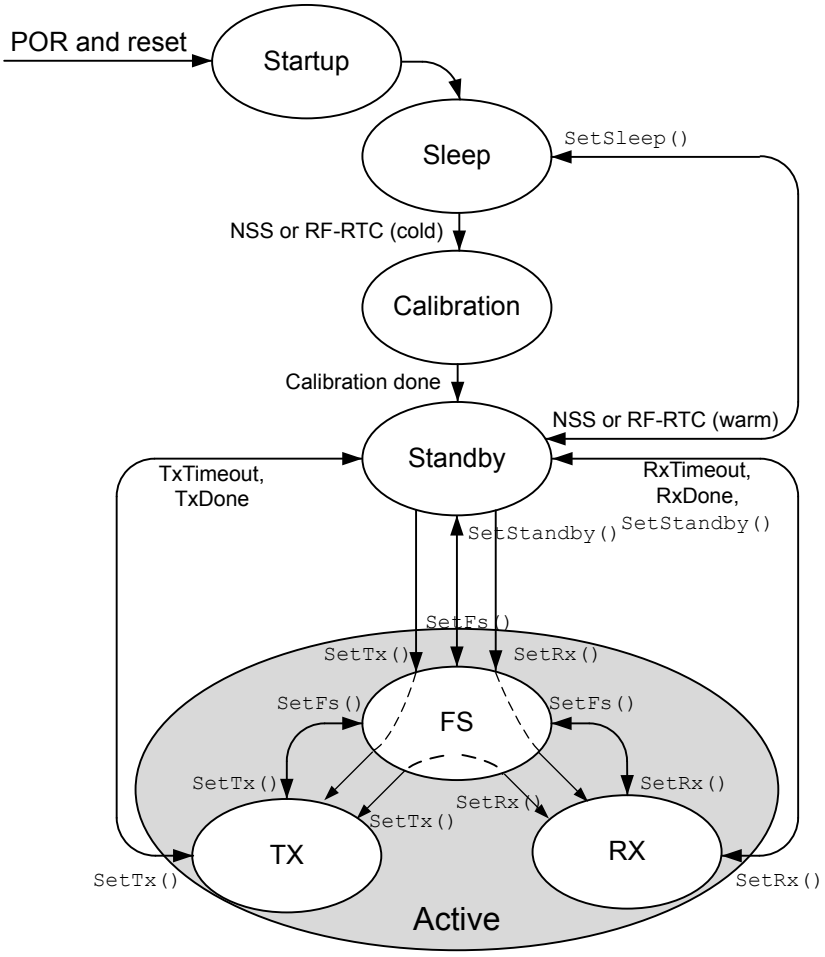
2.2 Sub-GHz radio operating modes

The sub-GHz radio implements the following power modes that behave independently from the system low-power modes described before:

- Sleep mode, reached when the RF communication is finished (consumption around 50 nA)
- Calibration mode, usually executed only once at boot (calibration results stored in RAM)
- Standby mode, transient state, before and after RF Rx/Tx operations, and before and after going into Sleep mode (reached by `SetSleep()` commend sent by the user). The consumption is between 0.7 to 1 mA.
- Active mode (Tx, Rx)

  Rx consumption varies from 4 to 10 mA, while Tx consumption varies from 15 to 120 mA, depending on various factors (such as frequency, transmit power or matching network).

Figure 6. Sub-GHz radio operating modes



Optimize the sub-GHz radio consumption is important, as the Rx consumption is 4 to 120 times greater than a typical CPU Run mode.

Some optimization factors are listed below:

- RF matching network (see the AN5457, *RF matching network design guide for STM32WL Series*)
- rate of the RF operations (application dependent)

The tables below detail the expected gain in function of the transmit (Tx) interval time.

Table 3. Stop 2 versus Standby gain, function of Tx interval time

Consumptions at 25 °C, 3 V, with SMPS and an optimized matching network.

Tx time (s)	Band[1]	Power amplifier	Tx power (dBm)	Tx time gain (in hh:mm)			
				1%	5%	10%	20%
1.48	High	High-power	22	0:37	3:08	6:24	13:15
			20	0:29	2:26	4:58	10:18
			17	0:18	1:32	3:07	6:27
			14	0:14	1:12	2:26	5:04
		Low-power	15	0:08	0:40	1:22	2:50
			14	0:07	0:37	1:15	2:37
			10	0:04	0:23	0:48	1:40
	Low	High-power	22	0:34	2:55	5:56	12:18
			20	0:22	1:54	3:52	8:01
			17	0:13	1:09	2:20	4:50
			14	0:11	1:00	2:02	4:14
		Low-power	15	0:07	0:38	1:19	2:43
			14	0:07	0:35	1:12	2:30
			10	0:04	0:20	0:42	1:26
0.7	High	High-power	22	0:17	1:29	3:01	6:16
			20	0:13	1:09	2:21	4:52
			17	0:08	0:43	1:28	3:03
			14	0:06	0:34	1:09	2:23
		Low-power	15	0:03	0:19	0:38	1:20
			14	0:03	0:17	0:35	1:14
			10	0:02	0:11	0:22	0:47
	Low	High-power	22	0:16	1:22	2:48	5:49
			20	0:10	0:54	1:49	3:47
			17	0:06	0:32	1:06	2:17
			14	0:05	0:28	0:58	2:00
		Low-power	15	0:03	0:18	0:37	1:17
			14	0:03	0:16	0:34	1:11
			10	0:01	0:09	0:19	0:41

1. *High = 868 to 915 MHz, Low = 434 to 490 MHz.*

Table 4. Stop 1 versus Stop 2 gain, function of Tx interval time

Consumptions at 25 °C, 3 V, with SMPS and an optimized matching network.

Tx time (s)	Band[1]	Power amplifier	Tx power (dBm)	Tx time gain (in hh:mm)			
				1%	5%	10%	20%
1.48	High	High-power	22	0:09	0:45	1:33	3:13
			20	0:07	0:35	1:12	2:30
			17	0:04	0:22	0:45	1:34
			14	0:03	0:17	0:35	1:13
		Low-power	15	0:01	0:09	0:20	0:41
			14	0:01	0:09	0:18	0:38
			10	0:01	0:05	0:11	0:24
	Low	High-power	22	0:08	0:42	1:26	2:59
			20	0:05	0:27	0:56	1:56
			17	0:03	0:16	0:34	1:10
			14	0:02	0:14	0:29	1:01
		Low-power	15	0:01	0:09	0:19	0:39
			14	0:01	0:08	0:17	0:36
			10	0:01	0:05	0:10	0:21
0.7	High	High-power	22	0:04	0:21	0:44	1:31
			20	0:03	0:16	0:34	1:11
			17	0:02	0:10	0:21	0:44
			14	0:01	0:08	0:16	0:34
		Low-power	15	0:00	0:04	0:09	0:19
			14	0:00	0:04	0:08	0:18
			10	0:00	0:02	0:05	0:11
	Low	High-power	22	0:03	0:20	0:41	1:24
			20	0:02	0:13	0:26	0:55
			17	0:01	0:07	0:16	0:33
			14	0:01	0:06	0:14	0:29
		Low-power	15	0:00	0:04	0:09	0:18
			14	0:00	0:04	0:08	0:17
			10	0:00	0:02	0:04	0:09

1. *High = 868 to 915 MHz, Low = 434 to 490 MHz.*

2.3 Power supplies

The STM32WL devices require a V_{DD} operating voltage supply between 1.8 V and 3.6 V, provided externally through VDD pins. V_{DD} is the external power supply for the I/Os, the sub-GHz radio, the internal regulator and the system analog functions (such as reset, power management and internal clocks).

An independent supply V_{DDA} can be provided for specific peripherals. This removes the need to supply the whole system with high voltage, when analog functions are used. Supplying the device with a low V_{DD} reduces the power consumption in low-power modes. When the peripherals supplied by V_{DDA} are not used in the application, V_{DDA} must be connected to V_{DD}.

In summary, the main power supplies are:

- V_{DD}, V_{DDRF}, and V_{DDSMPS}

  They all must be between 1.8 V to 3.6 V, and all connected together to the V_{DD}.
- V_{DDA} minimum voltage is:
  - 1.62 V for ADC and comparators
  - 2.4 V for the VREFBUF (built-in reference source)
  - 1.71 V for DAC without buffer and 1.8 V for the DAC with buffer

The STM32WL devices support also the voltage reference supply V_{REF+}, that is the input reference voltage for the ADC and DAC. V_{REF+} is also the output of the VREFBUF when enabled. The VREF+ pin, and thus internal reference voltage, is not available on all packages. When the VREF+ pin is double-bonded with the VDDA pin in a package, the internal reference voltage buffer is not available and must be kept disabled (refer to the product datasheet for pinout details).

To retain the content of the backup registers and to supply the RTC function when V_{DD} is turned off, the VBAT pin must be connected to an optional backup voltage V_{BAT}, supplied by a battery or by another source.

V_{BAT} must be between 1.55 to 3.6 V. It is the power supply for the RTC, TAMP, LSE and the backup registers (through power switch) when V_{DD} is not present. When V_{DD} is present, these peripherals (RTC, LSE) are automatically supplied by V_{DD}, and it is then possible to charge the external battery on V_{BAT} through an internal resistance.

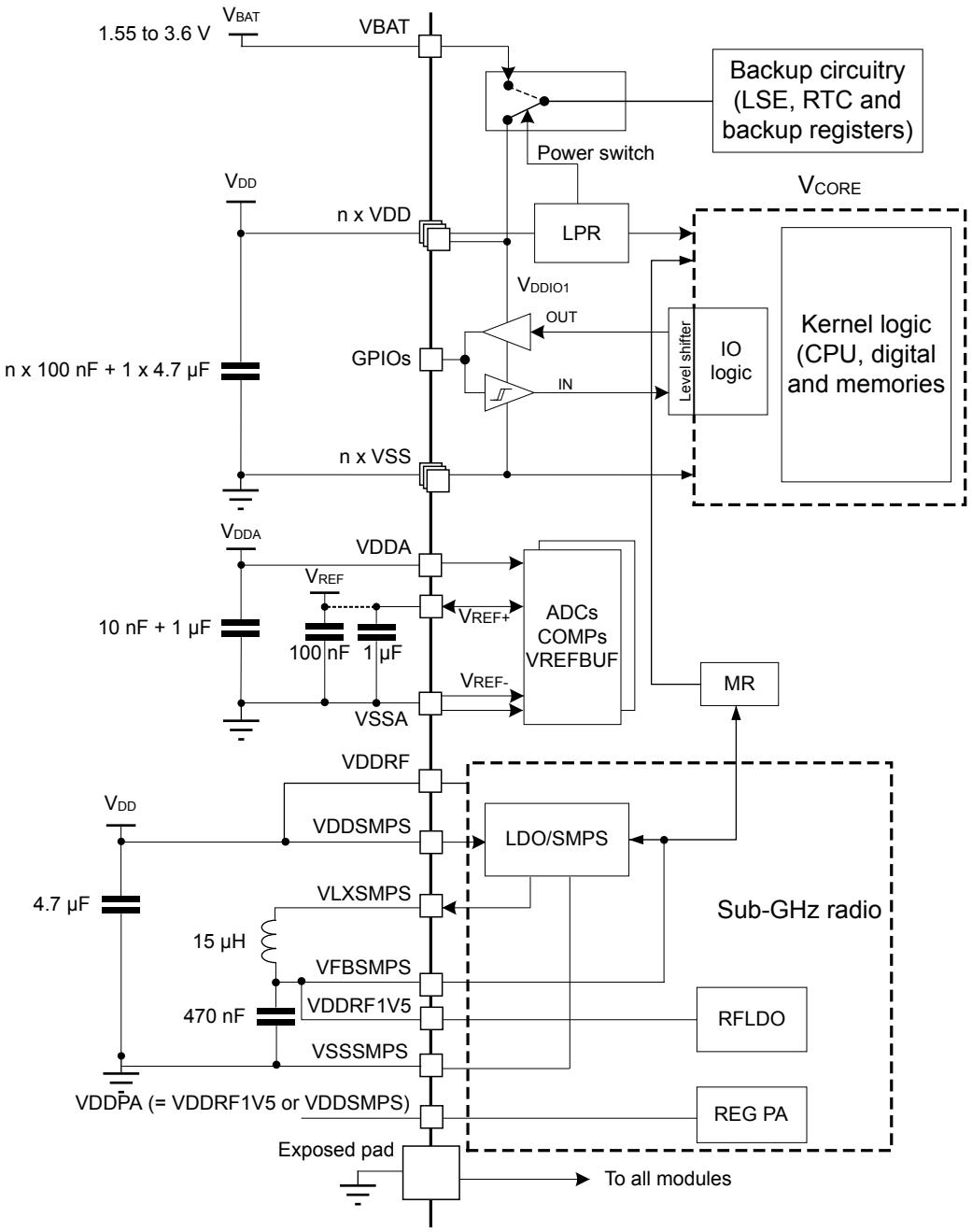
The STM32WL devices include a built-in SMPS to convert V_{DD} to the lowest voltage used by both the sub-GHz radio and the digital logic.

An embedded linear voltage regulator is used to supply the internal digital power V_{CORE}, that supplies the digital peripherals and memories. Thanks to the internal voltage regulator and voltage scaling, the power consumption in active modes is kept at a minimum, whatever the supply voltage.

Note:

- *Not all supply pins are present on all packages: refer to the product datasheet for details.*
- *When using independent voltage sources for VDDA, the power-on and power-off supply sequence must be compliant with the constraints specified in each product datasheet.*

Figure 7. **Power supply scheme**



SMPS

The STM32WL devices feature a switched-mode power supply (SMPS) to improve the power performance at high voltage. This SMPS supplies all the logic and RF power stages.

The SMPS can be used when the sub-GHz radio is active or in Sleep mode. The SMPS can be switched on/off on the fly, for examples if an analog task (such as an ADC acquisition) requires a very clean and stable supply.

The drive capability of the SMPS step-down converter can be controlled via a sub-GHz radio register. In reception or transmit high power, it is recommended to set 40 mA. In transmit low power, it is recommended to set 100 mA when 14/15 dBm, and 60 mA when below 14 dBm .

Note: The recommended SMPS coil is 15 µH. With a lower value, the application may suffer from disturbances introducing spurs on the RF output due to current and voltage variations.

2.4 Safe supply monitoring

The STM32WL devices include a sophisticated supply supervisor module with several programmable options. This module is active during both power-on/down and run-time phases.

The power-up is a critical phase where the various parts of the internal circuitry must be sequentially started and critical parameters (such as factory trimming values or options) are retrieved from the non-volatile memory to perform the device initialization, even before the user reset phase.

It is also during this period that V_{DD} can be impacted by glitches coming from the battery insertion or due to a weak power source.

The ultra-safe BOR circuitry guarantees that the reset is released only if the V_{DD} is above the selected threshold,whatever the slope of the V_{DD} ramp-up phase: the circuit is within its guaranteed operating conditions when the program execution starts.

A reset is generated when V_{DD} falls below the selected threshold. Five thresholds can be selected depending on the value stored in Flash memory option byte. The BOR minimum threshold is 1.8 V, guaranteeing that the device exits reset above 1.8 V, supplying 1.8 V ± 5% to the MCU.

The BOR is enabled in all modes except Shutdown mode, in which the power monitoring is disabled. As a consequence, the switch to V_{BAT} domain when V_{DD} is not present (and vice-versa) is not supported.

The radio end-of-life monitor provides information when V_{DD}t is too low to operate the sub-GHz radio. An interrupt can be generated when V_{DD} reaches the EOL level, to stop all radio activity in a safe way.

In addition, a 7-level programmable voltage detector (PVD) is available to generate an early interrupt in case of a voltage drop.

V_{DDA} is also monitored by comparing its value with a fixed voltage threshold. An interrupt is generated when V_{DDA} falls below the threshold.

The PVD and PVM(peripheral voltage monitor) can wakeup from Stop modes.

2.5 Peripherals tailored for low-power

The peripherals listed below require special attention, either because of their intrinsic high consumption, or because they are always powered up:

- Sub-GHz radio

  The STM32WL devices include a sub-GHZ radio that can be configured to work independently from system low-power mode selection. In listening mode, the sub-GHZ radio wakes up the device to perform an RF link operation. Once completed, the sub-GHZ radio automatically goes back to Sleep mode or wakes up the device if a packet is received.

- ADCs

  The STM32WL devices embed a multiple 12-bit/2.50 Msps ADC. This very fast and accurate converter can jeopardize the battery lifetime if left powered-up. As the ADC consumption is roughly proportional to the acquisition frequency (around 200 µA/Msps), from a consumption standpoint, the application can choose between the following solutions:

  – Perform the acquisition at low speed to limit the maximum current.

  – Perform the acquisition at the maximum speed to switch back to ultra-low-power mode quickly.

  When the acquisition is performed slowly, the ADC consumption itself can go down to few tens of a µA, drastically limiting the maximum current. This may be mandatory when the power source provides a limited current. If the CPU has no other task to perform during that time, this slow acquisition increases the time spent by the system in Run, Sleep, LPRun or LPSleep mode, versus the time spent in Stop or Standby ultra-low-power mode.

The following peripherals have been developed to operate even in Stop mode (when the system clock is stopped, with the main oscillator and the memory powered down):

- Ultra-low-power comparators

  Two comparators are available to monitor analog voltages and can wake up the device as soon as the external voltage reaches the selected threshold. These comparators can be combined together to provide a window comparator. One of these comparators has a rail-to-rail input capability and its output can be redirected to a timer for a general-purpose use.

- RTC

  This peripheral provides a clock/calendar with two alarms and includes a periodic wakeup unit plus several application specific functions (such as time-stamp and tamper detection). The RTC can remain enabled in the Shutdown mode, when most of the device is powered down. The RTC wakes up the full device circuitry in case of an event (such as an alarm or tamper detection). This peripheral also contains up to 80-byte backup registers to store contextual information when exiting from Standby mode, or to store sensitive information (protected by tamper detection mechanism and readout memory protection). The RTC has been designed using asynchronous design techniques to minimize its consumption.

  The RTC can be clocked by the following low-power low-speed clocks:

  – LSE: external 32.768 kHz quartz oscillator supporting four power consumption modes, combined with drive capability
  – LSI: internal 32 kHz oscillator that can clock the RTC with extremely low consumption, when high accuracy is not required

- LPTIM

  This peripheral is a 16-bit timer that benefits from the ultimate developments in power consumption reduction. With its clock source diversity, the LPTIM is able to keep running whatever the selected power mode. Given its capability to run even with no internal clock source, the LPTIM can be used as “pulse counter”, which can be useful in some applications. The LPTIM can also wake up the system from a low-power mode: this makes the LPTIM suitable with extremely low-power consumption “time-out functions”. This peripheral introduces a flexible clock scheme that provides the required functionality and performance, while minimizing the power consumption.

- LPUART

  This peripheral is a UART that allows bidirectional UART communications with a limited power consumption. The LSE is the only clock required to allow UART communications up to 9600 bauds. Higher baud rates can be reached when the LPUART is clocked by other sources. Even when the device is in Stop mode, the LPUART can wait for an incoming UART frame, while having an extremely low energy consumption.

  The following sources of wakeup from Stop mode can be selected:

  – wakeup on address match
  – wakeup on start bit detection
  – wakeup on received byte

- I2C

  This peripheral can wake up the device from Stop mode (APB clock is off), when it is addressed. All addressing modes are supported. To wakeup from Stop mode, the HSI must be selected as clock source for I2CCLK. During Stop mode, the HSI is switched off. When a start is detected, the I^2C interface switches the HSI on, and stretches the SCL clock pin low until the HSI wakes up. The HSI is then used for the address reception. In case of an address match, the I^2C stretches the SCL clock pin low during the device wakeup time. This stretch is released when the ADDR flag is cleared by software, and the transfer goes on normally. If the address does not match, the HSI is switched off again and the device is not woken up.

- USART

  This peripheral can wake up the device from Stop 0 or Stop 1 mode, when the USART clock is HSI or LSE. The following sources of wakeup from Stop0/1 mode can be selected:

  – wakeup on address match
  – wakeup on start bit detection
  – wakeup on received byte

All the available peripheral feature modes and wakeup capability are detailed in the product datasheet.

2.6 Versatile clock management

The RCC (reset and clock controller) peripheral manages the clock sources of the STM32WL devices. The following external oscillators can be used for applications requiring high precision:

- HSE (32 MHz high-speed external clock)

  Mandatory for RF operation, the HSE can be used to feed the PLL and to generate a CPU clock frequency of up to 48 MHz, and independent frequencies required for the audio clocks. This clock can be provided either by an external crystal, an external clock source or an external TCXO (temperature compensated crystal oscillator).
- LSE (32.768 kHz low-speed external clock)

  The LSE is normally used to provide a low-power clock source to the RTC (real time clock) and the sub-GHz radio. The LSE can also be used as LCD clock.

The following internal oscillators can be selected for various tasks:

- LSI (32 kHz low speed internal clock): ultra-low-power source that can feed the real-time clock (with a limited accuracy), the LCD controller and the IDWG
- HSI (16 MHz high speed internal clock): high speed voltage-compensated oscillator
- MSI (100 kHz to 48 MHz multi-speed internal clock): oscillator with an adjustable frequency and low current consumption, designed to operate with a current proportional to the frequency, so as to minimize the internal oscillator consumption overhead for the low CPU frequencies. This oscillator can provide a high-accuracy signal when configured in PLL-mode, where it is auto-calibrated using the LSE.

The table below summarizes the characteristics and uses of the various oscillators.

Table 5. Clock source characteristics for STM32WL devices

Clock source	Frequency	Consumption (typical)	Accuracy	Trimming	
				Factory	User
HSE (crystal)	32 MHz	50 µA	Crystal dependent, down to few ppm	NA	Yes (optional)
LSE	32.768 kHz (typical)	250 nA(1)	Crystal dependent, down to a few ppm	NA	
HSI	16 MHz	150 µA	± 0.8 % typical over -10 to +85 °C +0.1/-0.2 % typical over 1.8 V to 3.6 V	Yes	Yes
MSI	100 kHz 200 kHz 400 kHz 800 kHz 1 MHz 2 MHz 4 MHz 8 MHz 16 MHz 24 MHz 32 MHz 48 MHz	0.6 µA 0.8 µA 1.2 µA 1.9 µA 4.7 µA 6.5 µA 11 µA 18.5 µA 62 µA 85 µA 110 µA 155 µA	Default mode: +1.5/-1 % typical over -10 to +85 °C +1.5/-5.5 % typical for 16 to 48 MHz over 1.62 to 3.6 V PLL-mode: less than 0.25 %	Yes	Yes
LSI	32 kHz	110 nA	±1.5 % typical over -40 to +125 °C +0.5/-1.5 % typical over 1.8 V to 3.6 V	Yes	No

1. *Consumption is dependent of the LSE oscillator drive capability (here for low drive). At 25° C/3 V, medium-low, medium-high and high drive capability consumes respectively around 25%, 100% and 150% more than low drive (see AN2867 for more information to understand which drive capability can be used, function of the selected XO).*

In addition, the STM32WL devices embed one PLL, that provides up to three independent outputs, and can be fed by the HSI, the HSE or the MSI. These PLL outputs can be configured independently for the system clock or the ADC interface clock . This removes the peripheral constraints on the system clock.

Many other peripherals can be clocked independently from the system clock: USART, LPUART, I2Cx (x = 1 to 3) and LPTIMx (x = 1, 2) receive an independent clock. For instance, the system and APB bus frequencies can be reduced while keeping the communication peripheral baud rate constant, independently of the system clock frequency.

All peripheral clocks can be individually enabled or disabled in Run and LPRun modes. The peripheral clocks can also be individually enabled or disabled in Sleep and LPSleep modes.

Although the HSI and the MSI are factory trimmed, they can be further trimmed in 0.5% steps during run time, to compensate frequency deviations due to temperature and voltage changes.

When the LSE is present in the application, the MSI can be automatically calibrated using the LSE (PLL-mode configuration), in order to reach long-term LSE accuracy.

When the device exits from Stop mode, the system clock can be configured to be either HSI or MSI at any frequency range. This enables the exit from Stop mode directly at 48 MHz.

3 Conclusion

The main features of the STM32WL devices presented in this application note, demonstrate the benefits offered by this microcontroller family in reducing the current consumption in embedded communication systems.

Besides having the same characteristics of the STM32WB Series or STM32L4 Series microcontrollers, the STM32WL devices offer high processing performance without compromising the power consumption. They complement the STM32 portfolio, maintaining compatibility with other STM32 devices.

The rich set of peripherals, associated with the ultra-low-power sub-GHz radio, allows the user to cover a wide range of applications, while the available low-power modes give full flexibility to adjust the consumption for any task on the fly.

This results in an extended operating lifetime for today and tomorrow constantly greener applications.

Revision history

Table 6. **Document revision history**

Date	Version	Changes
30-Nov-2020	1	Initial release.
4-May-2021	2	Added note at the end of Section 2.3 Power supplies.

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