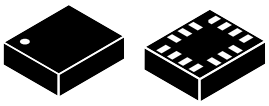
Ultra-wide bandwidth, low-noise 3-axis digital accelerometer



LGA-14L
(2.5 x 3.0 x 0.83 mm) typ.

Features

- 3-axis accelerometer with digital output
- User-selectable full-scale: ±2/±4/±8/±16 *g*
- Ultra-wide and flat frequency response range: from dc to 5 kHz (±3 dB point)
- Ultra-low noise density: down to 90 µg/√Hz in 3-axis mode / 65 µ*g*/√Hz in single-axis mode
- High stability of the sensitivity over temperature and against mechanical shock
- Extended temperature range from -40 to +105 °C
- Low power: 1.1 mA with all 3 axes delivering full performance
- SPI serial interface
- Low-pass or high-pass filter with selectable cut-off frequency
- Interrupts for wake-up / vibration - no vibration / FIFO thresholds
- Embedded FIFO: 3 kB
- Embedded temperature sensor
- Embedded self-test
- Supply voltage: 2.1 V to 3.6 V
- Compact package: LGA 2.5 x 3 x 0.83 mm 14-lead
- ECOPACK®, RoHS and “Green” compliant

Product status link
IIS3DWB

Product summary	
Order code	IIS3DWBTR
Temperature range [°C]	-40 to +105
Package	LGA-14
Packing	Tape and reel

Product label

Applications

- Vibration monitoring
- Condition monitoring
- Predictive maintenance
- Test and measurements

Description

The IIS3DWB is a system-in-package featuring a 3-axis digital accelerometer with low noise over an ultra-wide and flat frequency range. The wide bandwidth, low noise, very stable and repeatable sensitivity, together with the capability of operating over an extended temperature range (up to +105 °C), make the device particularly suitable for vibration monitoring in industrial applications.

The high performance delivered at low power consumption, together with the digital output and the embedded digital features like the FIFO and the interrupts are enabling features for battery-operated industrial wireless sensor nodes.

The IIS3DWB has a selectable full-scale acceleration range of ±2/±4/±8/±16 g and is capable of measuring accelerations with a bandwidth up to 5 kHz with an output data rate of 26.7 kHz. A 3 kB first-in, first-out (FIFO) buffer is integrated in the device to avoid any data loss and to limit intervention of the host processor.

The MEMS sensor module family from ST leverages the robust and mature manufacturing processes already used for the production of micromachined accelerometers and gyroscopes to serve automotive, industrial and consumer markets. The sensing elements are manufactured using ST’s proprietary

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micromachining process, while the embedded IC interfaces are developed using CMOS technology.

The IIS3DWB has a self-test capability which allows checking the functioning of the sensor in the final application. The IIS3DWB is available in a 14-lead plastic land grid array (LGA) package and is guaranteed to operate over an extended temperature range from -40 °C to +105 °C.

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1 Pin description

Figure 1. **Pin connections**

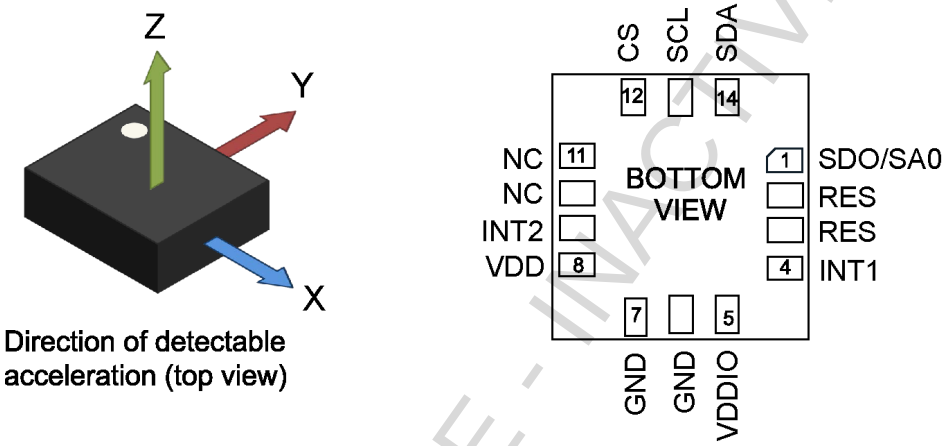

Table 1. **Pin desription**

Pin #	Name	Function
1	SDO/SA0	SPI 4-wire interface serial data output (SDO) I²C(1) least significant bit of the device address (SA0)
2	RES	Connect to VDDIO or GND
3	RES	Connect to VDDIO or GND
4	INT1	Programmable interrupt 1
5	Vdd_IO(2)	Power supply for I/O pins
6	GND	Connect to GND
7	GND	Connect to GND
8	Vdd(3)	Power supply
9	INT2	Programmable interrupt 2
10	NC	Connect to Vdd_IO or leave unconnected(4)
11	NC	Connect to Vdd_IO or leave unconnected(4)
12	CS	I²C/SPI(1) mode selection (1: SPI idle mode / I²C(1) communication enabled; 0: SPI communication mode / I²C(1) disabled)
13	SCL	I²C serial clock (SCL) SPI serial port clock (SPC)
14	SDA	I²C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)

1. *I²C can be used only in single-axis mode or for debugging.*
2. *Recommended 100 nF filter capacitor.*
3. *Recommended 100 nF plus 10 µF capacitors.*
4. *Leave pin electrically unconnected and soldered to PCB.*

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2 Module specifications

2.1 Mechanical characteristics

@ Vdd = 3.0 V, T = 25 °C unless otherwise noted. The product is factory calibrated at 3.0 V. The operational power supply range is from 2.1 V to 3.6 V.

Table 2. Mechanical characteristics

Symbol	Parameter	Test conditions	Min. (1)	Typ. (2)	Max.(1)	Unit
FS	Linear acceleration measurement range			±2		*g*
				±4		
				±8		
				±16		
So	Linear acceleration sensitivity(3)	FS = ±2 *g*		0.061		mg/LSB
		FS = ±4 *g*		0.122		
		FS = ±8 *g*		0.244		
		FS = ±16 *g*		0.488		
BW	Signal bandwidth	±3 dB point	5			kHz
ODR	Linear acceleration output data rate			26.667		kHz
F0	Sensor resonant frequency			7.0		kHz
Top	Operating temperature range		-40		+105	°C

1. *Min/Max values are based on characterization results at 3σ, not tested in production and not guaranteed*
2. *Typical specifications are not guaranteed.*
3. *Sensitivity values after factory calibration test and trimming.*

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2.2 Electrical characteristics

@ Vdd = 3.0 V, T = 25 °C unless otherwise noted.

Table 3. Electrical characteristics

Symbol	Parameter	Test conditions	Min.(1)	Typ. (2)	Max.(1)	Unit
Vdd	Supply voltage		2.1		3.6	V
Vdd_IO	Power supply for I/O		1.62		Vdd + 0.1	V
Idd	Accelerometer current consumption	ODR = 26.7 kHz		1.1		mA
IddPD	Accelerometer current consumption during power-down			3		µA
Ton	Turn-on time(3)			10		ms
V_{IH}(4)	Digital high-level input voltage		0.7 *VDD_IO			V
V_{IL}(4)	Digital low-level input voltage				0.3 *VDD_IO	V
V_{OH}(4)	High-level output voltage	I_{OH} = 4 mA(5)	VDD_IO - 0.2			V
V_{OL}(4)	Low-level output voltage	I_{OL} = 4 mA(5)			0.2	V
Top	Operating temperature range		-40		+105	°C

1. *Min/Max values are based on characterization results at 3σ, not tested in production and not guaranteed.*
2. *Typical specifications are not guaranteed.*
3. *Time to obtain valid data switching from power-down to normal operation.*
4. *Guaranteed by design characterization and not tested in production.*
5. *4 mA is the maximum driving capability, i.e. the maximum DC current that can be sourced/sunk by the digital pad in order to guarantee the correct digital output voltage levels V_{OH} and V_{OL}.*

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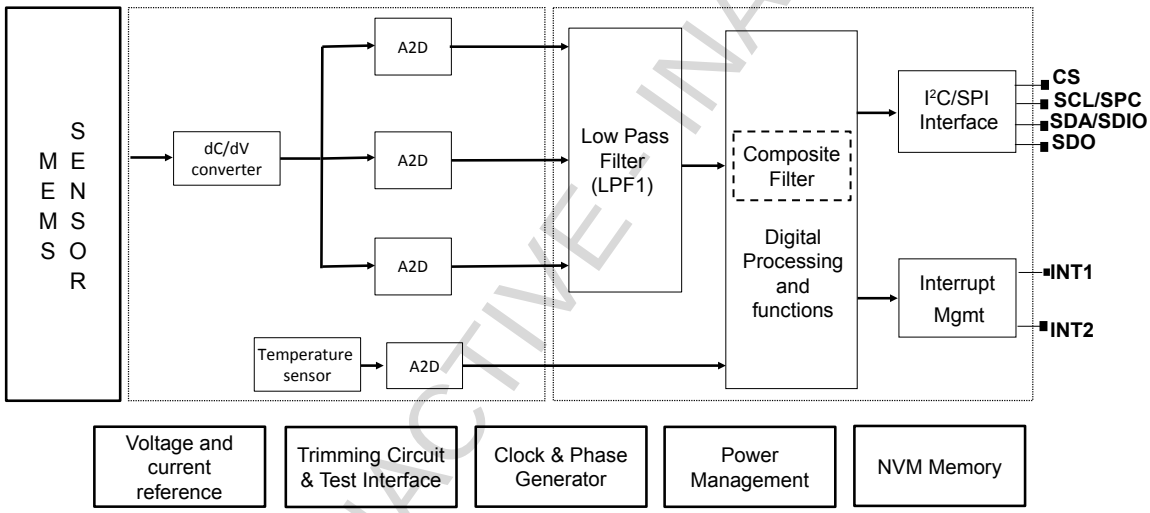
3 Block diagram

The IIS3DWB architecture is composed of the following functional blocks:

- MEMS mechanical element
- ADC
- digital filter (LPF1)
- composite filter

Figure 2. Accelerometer architecture



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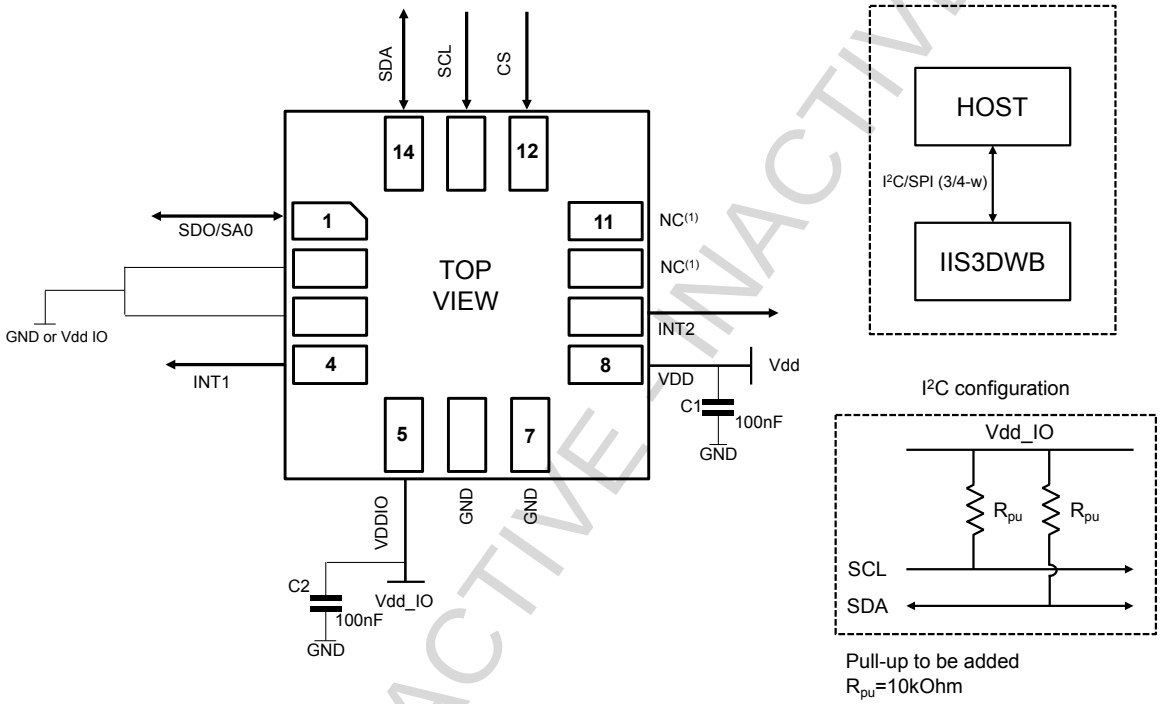
4 IIS3DWB electrical connections

Figure 3. **IIS3DWB electrical connections**



The device core is supplied through the Vdd line while the I/O pads are supplied through the Vdd_IO line. Power supply decoupling capacitors (C1, C2 = 100 nF ceramic) should be placed as near as possible to the the supply pin of the device (common design practice).

The functionality of the device and the measured acceleration data are selectable and accessible through the I²C or SPI interfaces. When using the I²C protocol, CS must be tied high. Every time the CS line is set to low level, the I²C bus is internally reset.

All the functions, the threshold and the timing of the two interrupt pins can be completely programmed by the user through the I²C/SPI interface.

Note: I²C can be used only in single-axis mode or for debugging .

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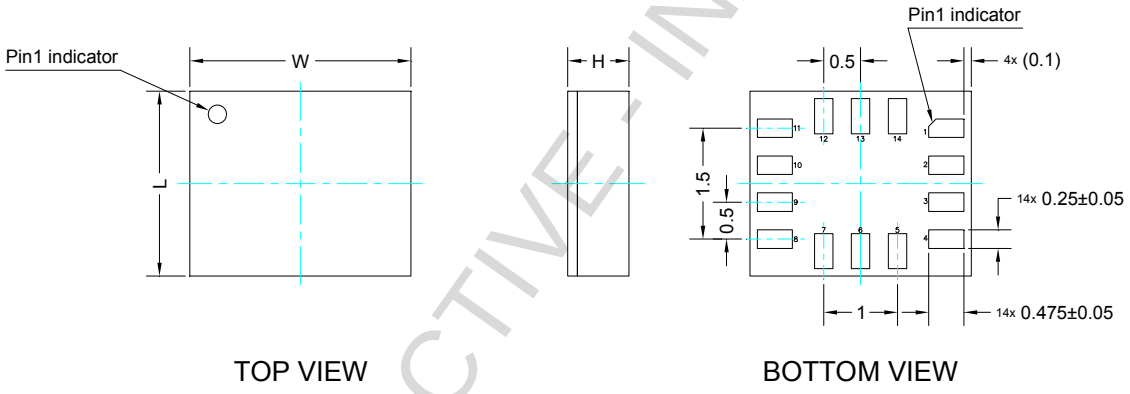
5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

5.1 LGA-14L package information

Figure 4. LGA-14L 2.5 x 3.0 x 0.83 mm³ (typ) package outline and mechanical data



Dimensions are in millimeter unless otherwise specified
General tolerance is +/-0.1mm unless otherwise specified

OUTER DIMENSIONS

ITEM	DIMENSION [mm]	TOLERANCE [mm]
Length [L]	2.50	±0.1
Width [W]	3.00	±0.1
Height [H]	0.86	MAX

DM00249496_1

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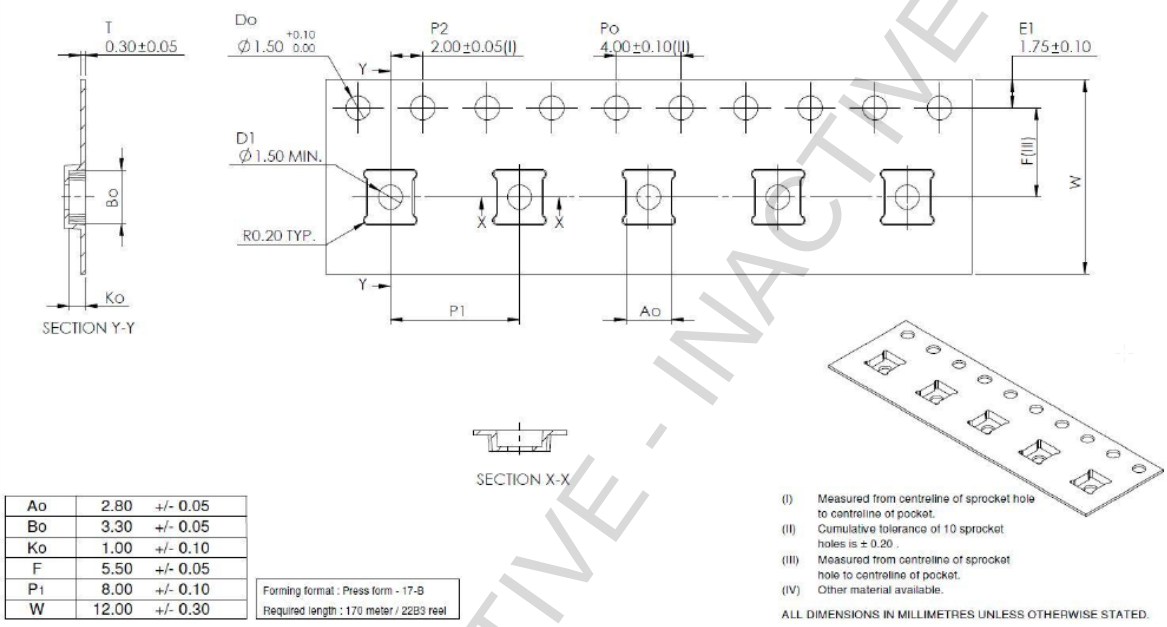
5.2 LGA-14 packing information

Figure 5. Carrier tape information for LGA-14 package



Ao	2.80	+/- 0.05
Bo	3.30	+/- 0.05
Ko	1.00	+/- 0.10
F	5.50	+/- 0.05
P1	8.00	+/- 0.10
W	12.00	+/- 0.30

Forming format : Press form - 17-B
Required length : 170 meter / 2283 reel

Figure 6. LGA-14 package orientation in carrier tape

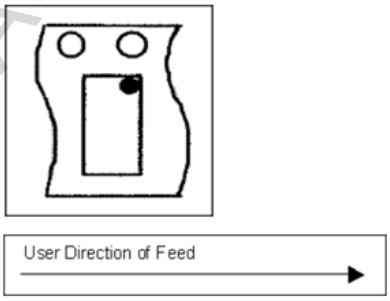


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Figure 7. **Reel information for carrier tape of LGA-14 package**

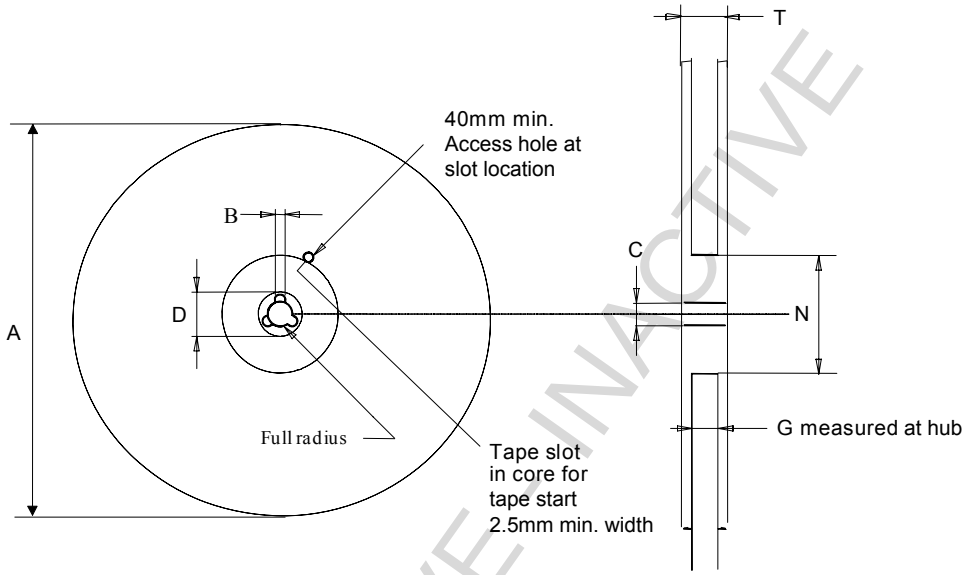

Table 4. **Reel dimensions for carrier tape of LGA-14 package**

Reel dimensions (mm)	
A (max)	330
B (min)	1.5
C	13 ±0.25
D (min)	20.2
N (min)	60
G	12.4 +2/-0
T (max)	18.4

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Revision history

Table 5. **Document revision history**

Date	Version	Changes
15-Nov-2018	1	Initial release

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