UM2702

User manual

1200 W motor control power board based on STIB1060DM2T-L SLLIMM™ 2nd series MOSFET IPM

Introduction

The STEVAL-IPMM10B is a compact motor drive power board equipped with SLLIMM™ (small low-loss intelligent molded module) 2nd series based on n-channel power MOSFET MDmesh™ DM2 fast-recovery diode (STIB1060DM2T-L). It provides an affordable and easy-to-use solution for driving high power motors for a wide range of applications such as power white goods, air conditioning, compressors, power fans, high-end power tools and 3-phase inverters for motor drives in general. The IPM itself consists of MOSFETs and a wide range of features like undervoltage lockout, smart shutdown, embedded temperature sensor and NTC, and overcurrent protection.

The main characteristics of this evaluation board are small size, minimal BOM and high efficiency. It consists of an interface circuit (BUS and VCC connectors), bootstrap capacitors, snubber capacitor, hardware short-circuit protection, fault event and temperature monitoring. In order to increase the flexibility, it is designed to work in single- or three-shunt configuration and with double current sensing options such as using three dedicated onboard op-amps, or op-amps embedded in the MCU. The Hall/ Encoder part completes the circuit.

Thanks to these advanced characteristics, the system has been specifically designed to achieve fast and accurate current feedback conditioning, satisfying the typical requirements for field-oriented control (FOC).

The STEVAL-IPMM10B is compatible with ST's STM32-based control board, enabling designers to build a complete platform for motor control.

Figure 1. SLLIMM 2nd series motor control internal demo board (top view)

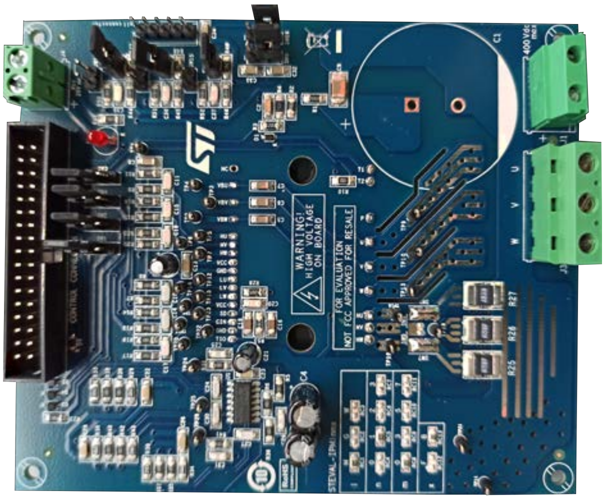
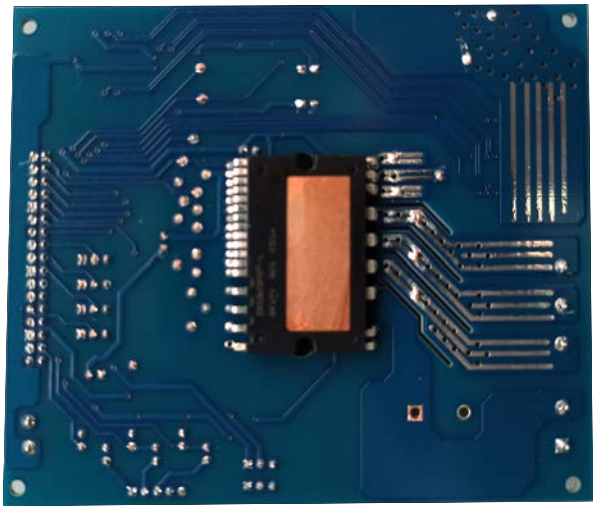


Figure 2. SLLIMM 2nd series motor control internal demo board (bottom view)



1 Key features

- Input voltage: 125 - 400 VDC
- Nominal power: up to 1200 W
  - Allowable maximum power is related to the application conditions and cooling system
- Nominal current: up to 4.2 A_{rms}
- Input auxiliary voltage: up to 20 V DC
- Single- or three-shunt resistors for current sensing (with sensing network)
- Two options for current sensing: dedicated op-amps or through MCU
- Overcurrent hardware protection
- IPM temperature monitoring and protection
- Hall sensor or encoder input
- MOSFET intelligent power module:
  - SLLIMM™ 2nd series IPM (STIB1060DM2T-L - DBC package)
- Motor control connector (32-pin) to interface with ST MCU boards
- Universal conception for further evaluation with breadboard and testing pins
- Very compact size
- WEEE compliant
- RoHS compliant

2 Circuit schematics

The full schematics for the SLLIMM™ 2nd series card for STIB1060DM2T-L IPM products is shown below. This card consists of an interface circuit (BUS and V_{CC} connectors), bootstrap capacitors, snubber capacitor, shortcircuit protection, fault output circuit, temperature monitoring, single-/three-shunt resistors and filters for input signals. It also includes bypass capacitors for V_{CC} and bootstrap capacitors. The capacitors are located very close to the drive IC to avoid malfunction due to noise.

Dual current sensing options are provided: three dedicated on-board op-amps or embedded MCU op-amps; selection is performed through three jumpers.

The Hall/Encoder section (powered at 5 V or 3.3 V) completes the circuit.

2.1 Schematic diagrams

Figure 3. **STEVAL-IPMM10B board schematic (1 of 5)**

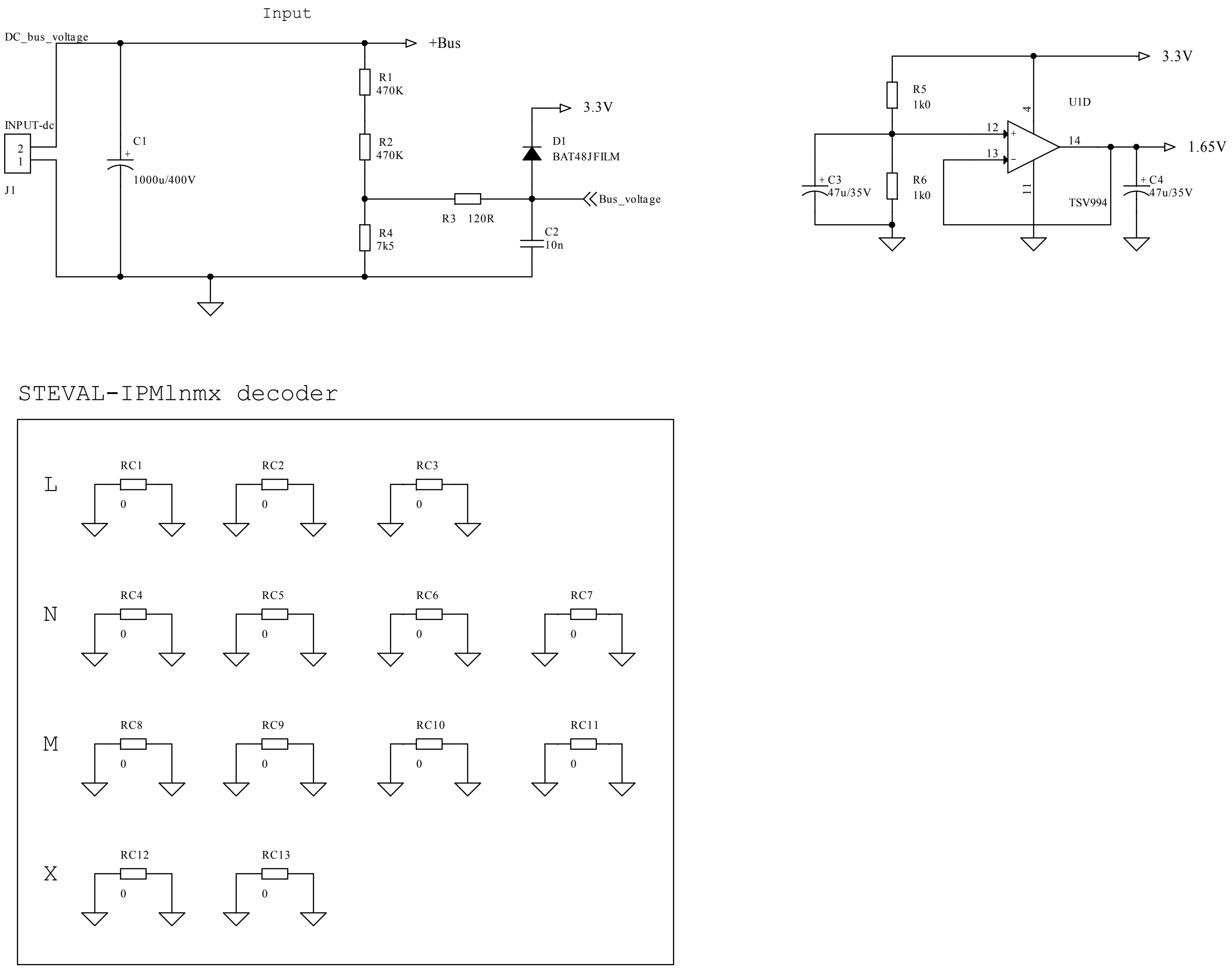


Figure 4. **STEVAL-IPMM10B board schematic (2 of 5)**

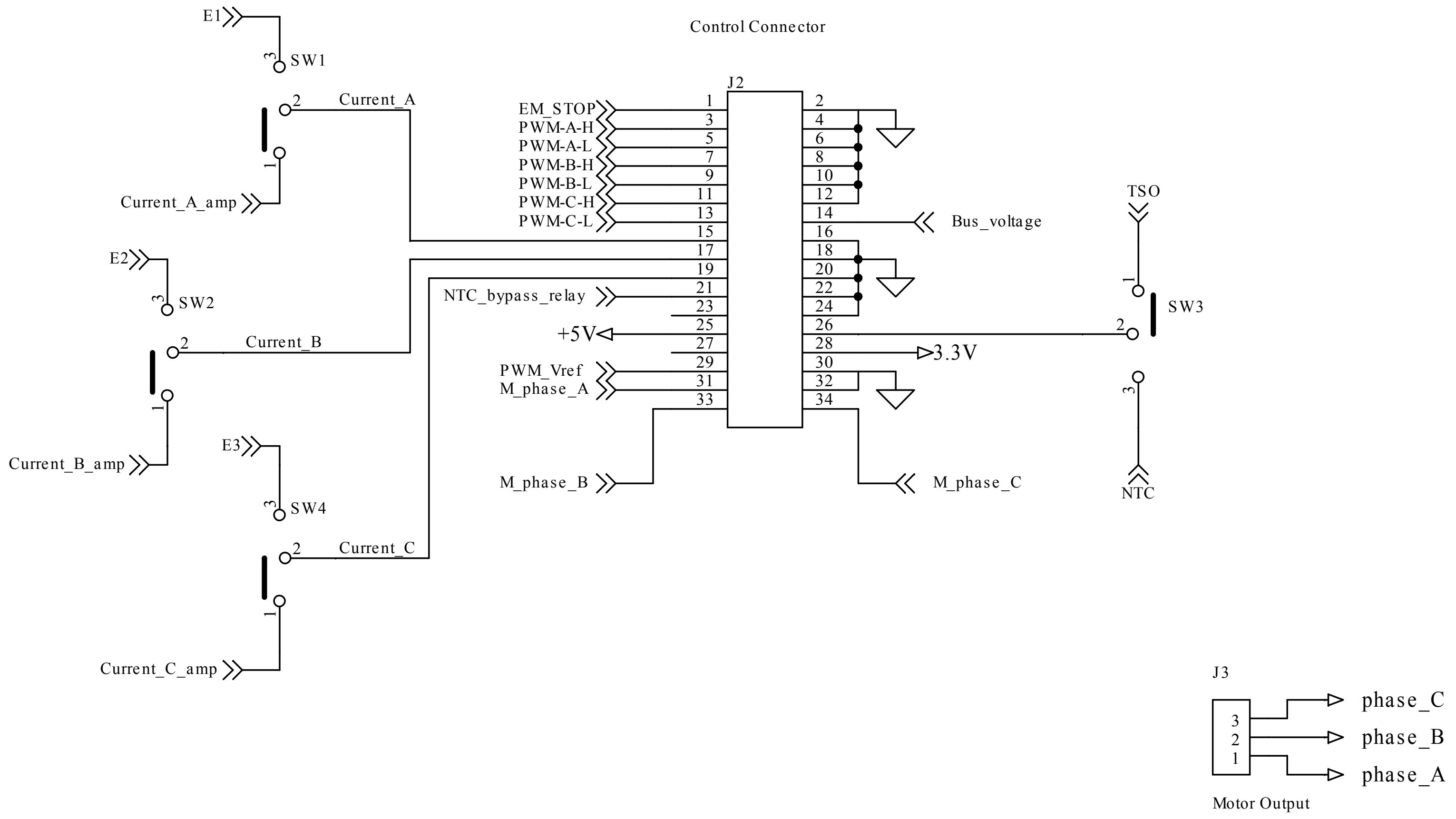


Figure 5. **STEVAL-IPMM10B board schematic (3 of 5)**

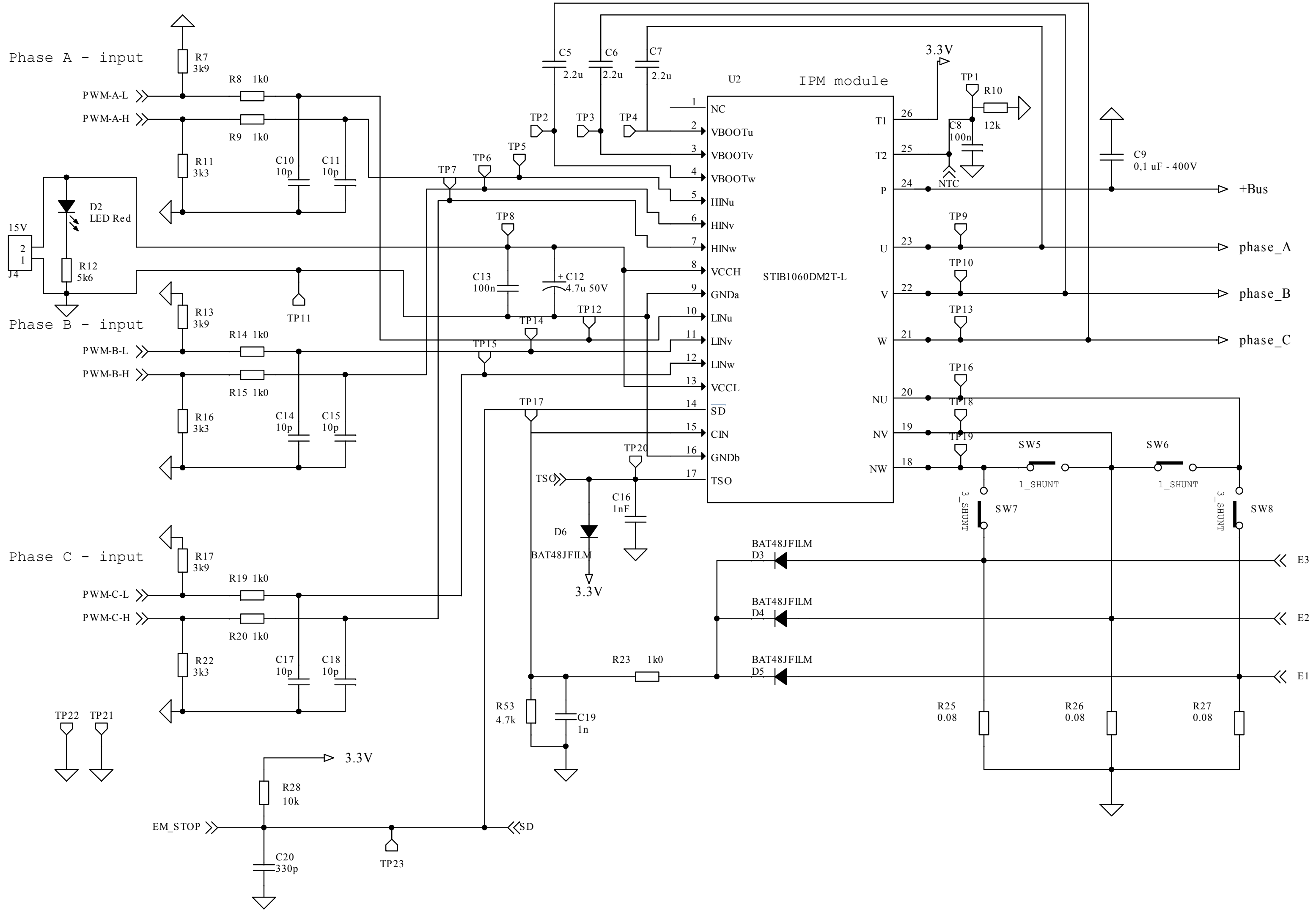


Figure 6. **STEVAL-IPMM10B board schematic (4 of 5)**

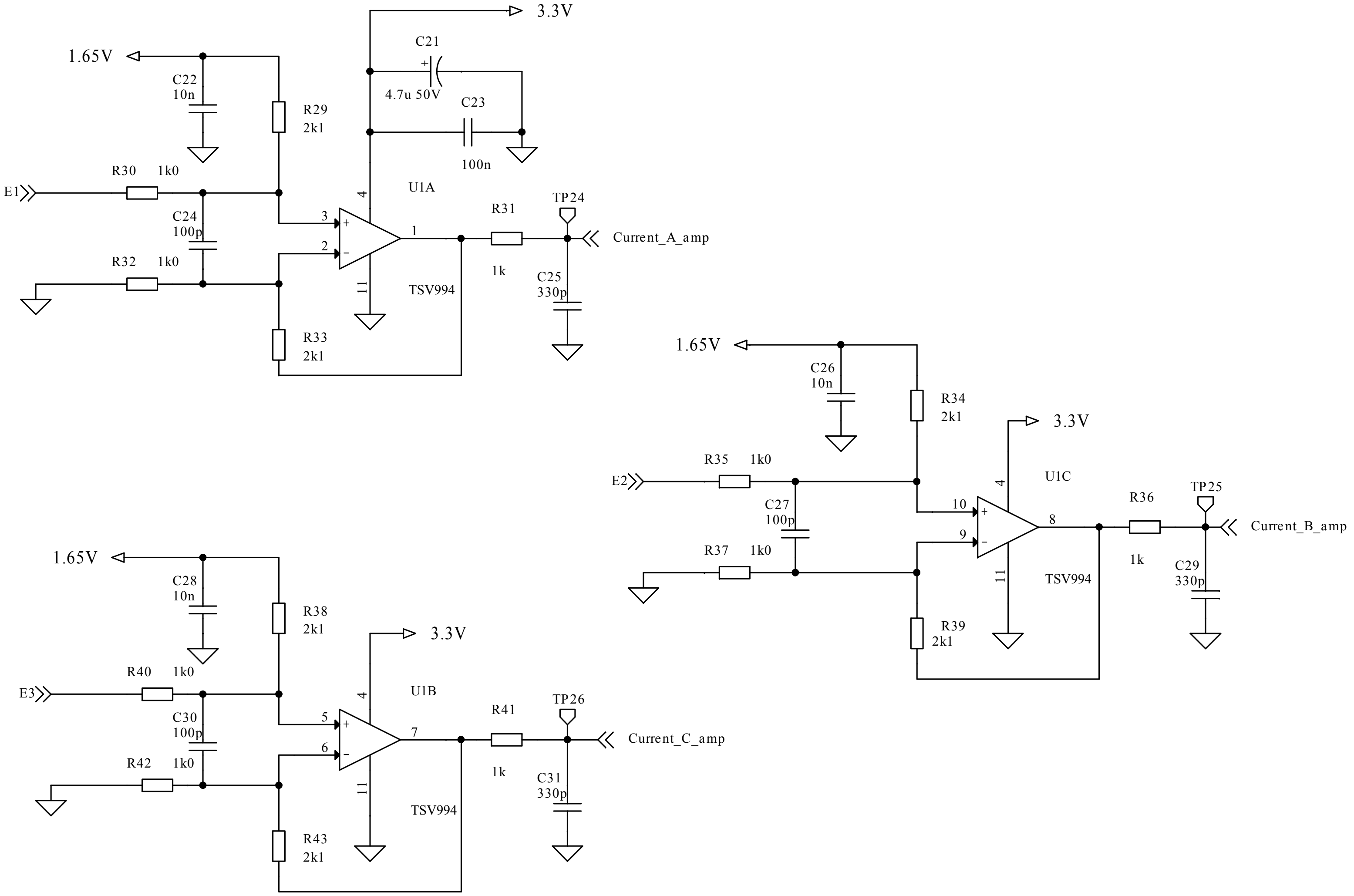
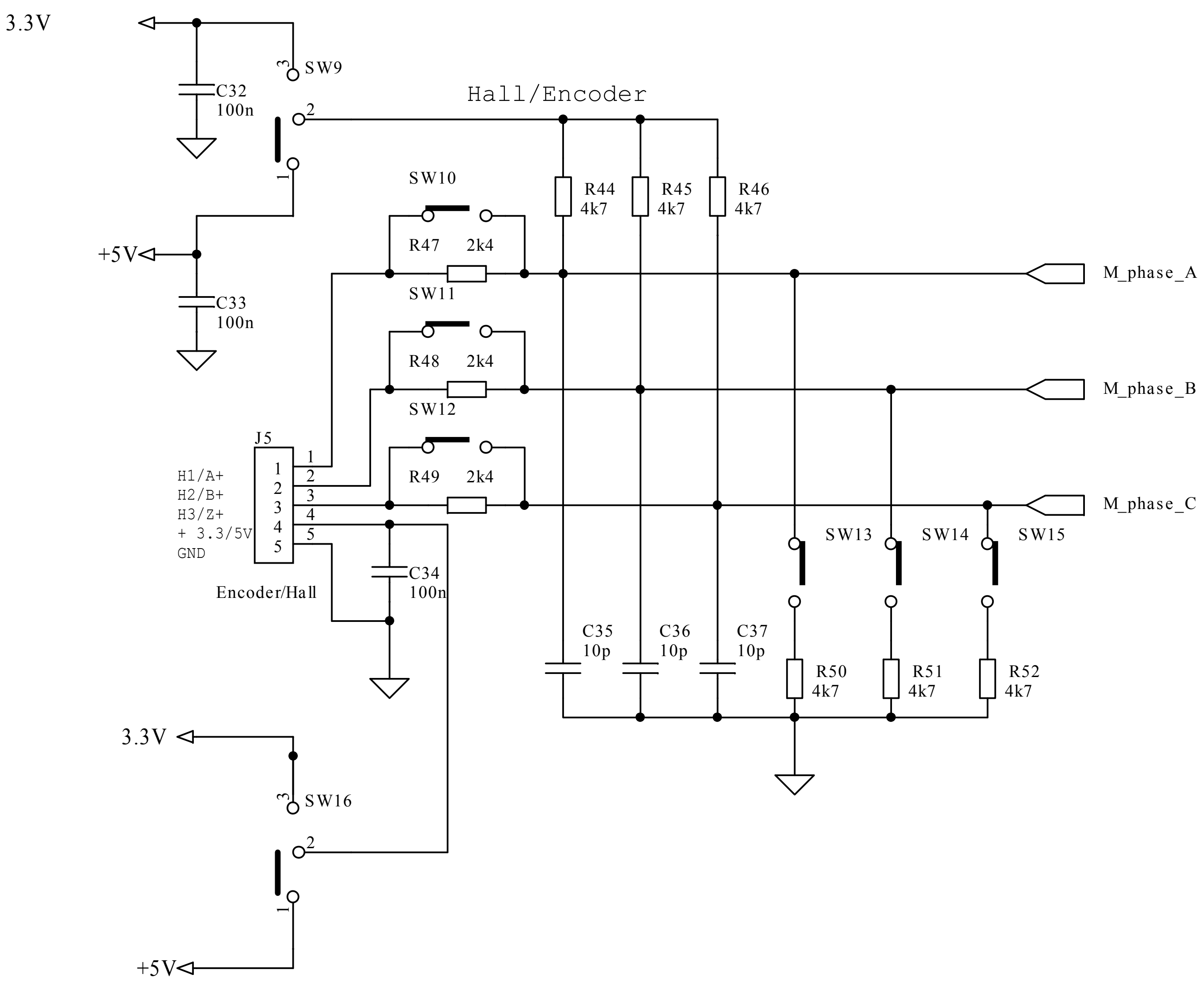


Figure 7. **STEVAL-IPMM10B board schematic (5 of 5)**



3 Main characteristics

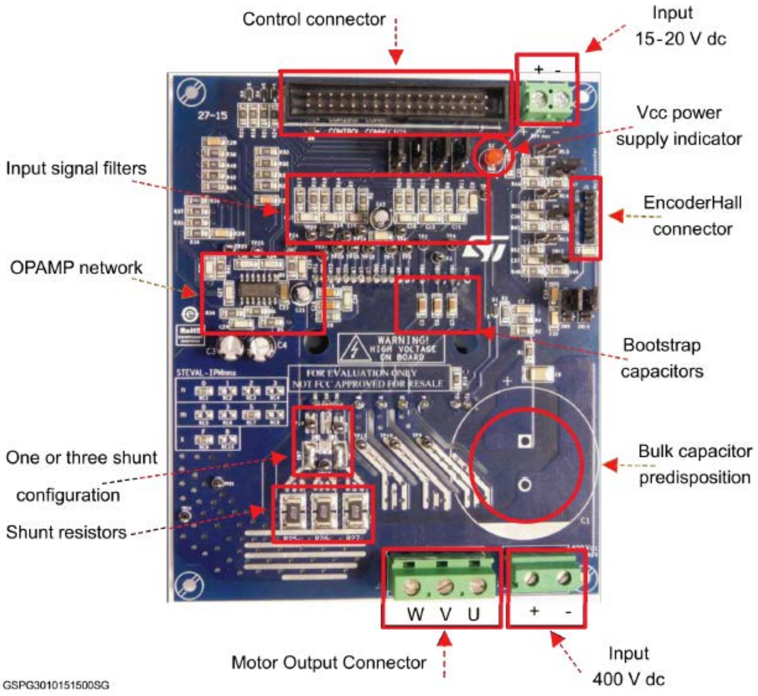
The board is designed to be compatible with DC supply from 125 VDC up to 400 VDC voltage.

A bulk capacitor according to the power level of the application must be mounted. The footprint is already provided on the board.

The SLLIMM integrates six MOSFET switches with high voltage gate drivers. Thanks to this integrated module, the system is specifically designed to achieve power inversion in a reliable and compact design. Such integration reduces the required PCB area and the simplicity of the design increases reliability.

In order to increase the flexibility, it can operate in single- or three-shunt configuration by modifying solder bridge jumper settings (see Section 4.3.5 Single- or three-shunt selection).

Figure 8. **STEVAL-IPMM10B architecture**



4 Filters and key parameters

4.1 Input signals

The input signals (LINx and HINx), able to drive the internal MOSFETs, are active high. A 100 kΩ (typ.) pull-down resistor is built-in for each input signal. In order to prevent input signal oscillation, an RC filter was added on each input and placed as close as possible to the IPM. The filter is designed using a time constant of 10 ns (1 kΩ and 10 pF).

4.2 Bootstrap capacitor

In the 3-phase inverter, the emitters of the low side MOSFETs are connected to the negative DC bus (VDC-) as common reference ground, which allows all low side gate drivers to share the same power supply, while the emitter of high side MOSFETs is alternately connected to the positive (VDC+) and negative (VDC-) DC bus during running conditions.

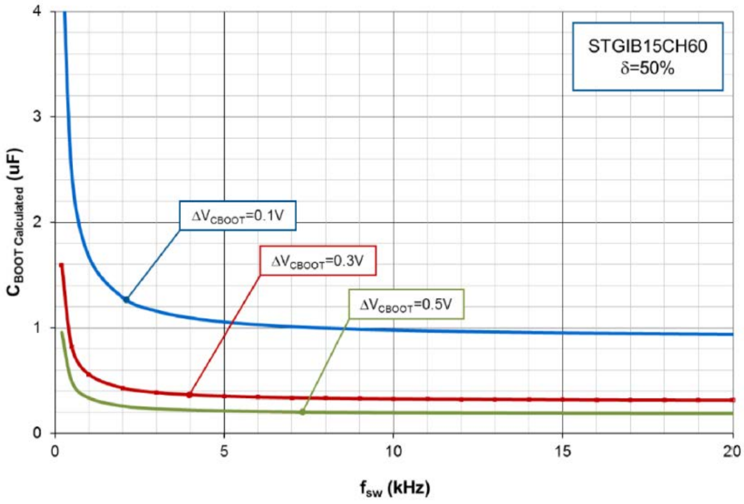
A bootstrap method is a simple and cheap solution to supply the high voltage section. This function is normally accomplished by a high voltage fast recovery diode. The SLLIMM 2nd series family includes a patented integrated structure that replaces the external diode. It is realized with a high voltage DMOS functioning as diode with series resistor. An internal charge pump provides the DMOS driving voltage. The value of the CBOOT capacitor should be calculated according to the application condition.

This curve is taken from application note AN4768 (available on www.st.com); calculations are based on the STGIB15CH60TS-L device, which represents the worst case scenario for this kind of calculation.

Figure Figure 9. C_{BOOT} graph selectiongraph selection shows the behavior of CBOOT (calculated) versus switching frequency (fsw), with different values of ΔVCBOOT for a continuous sinusoidal modulation and a duty cycle δ = 50%.

The boot capacitor must be two or three times larger than the CBOOT calculated in the graph. For this design, a value of 2.2 μF was selected.

Figure 9. C_{BOOT} graph selection



4.3 Overcurrent protection

The SLLIMM 2nd series integrates a comparator for fault sensing purposes. The comparator has an internal voltage reference VREF (510 mV typ.) connected to the inverting input, while the non-inverting input available on the CIN pin can be connected to an external shunt resistor to implement the overcurrent protection function.

When the comparator triggers, the device enters the shutdown state.

The comparator output is connected to the SD pin in order to send the fault message to the MCU.

4.3.1 SD Pin

The $\overline{\text{SD}}$ is an input/output pin (open drain type if used as output). Taking into account the voltage reference on SD (3.3 V), a pull up resistor of 10 kΩ (R28) is used to guarantee the right bias and consequently to keep the current on the open drain DMOS (Iod) lower than 3 mA.

The filter on $\overline{\text{SD}}$ (R28 and C20) has to be sized to obtain the desired re-starting time after a fault event and placed as close as possible to the $\overline{\text{SD}}$ pin.

A shutdown event can be managed by the MCU, in this case the $\overline{\text{SD}}$ functions as the input pin.

Conversely, the $\overline{\text{SD}}$ functions as an output pin when an overcurrent or undervoltage condition is detected.

4.3.2 Fault management

The SLLIMM 2nd series integrates a specific kind of fault management, useful when SD is functioning as output, able to identify the type of fault event.

As previously described, as soon as a fault occurs, the open-drain (DMOS) is activated and LVGx outputs are forced low.

Two types of fault can be signaled:

- Overcurrent (OC) sensed by the internal comparator (CIN);
- Undervoltage (UVLO) on supply voltage (VCC).

Each fault enables the SD open drain for a different time (see the table below).

The duration of a shutdown event therefore tells us the type of failure that has occurred.

Table 1. **Fault timing**

Symbol	Parameter	Event time	SD open-drain enable time result
OC	Overcurrent event	≤ 24 µs	24 µs
		> 24 µs	OC time
UVLO	Undervoltage lockout event	≤ 70 µs	70 µs
		> 70 µs until VCC_LS exceeds the VCC_LS UV turn on threshold	UVLO time

Note: *typical value (TJ = -40 °C to 125 °C)*

Note: *without contribution of RC network on SD*

Figure 10. SD failure due to overcurrent shows a shutdown as the result of an overcurrent event. During the overcurrent, the voltage on the comparator (CIN) exceeds the threshold (0.51 V typ.) and the shutdown is able to stop the application. In this case, the SD event time is about 24 µs (for OC event less than 24 µs).

Figure 10. **SD failure due to overcurrent**

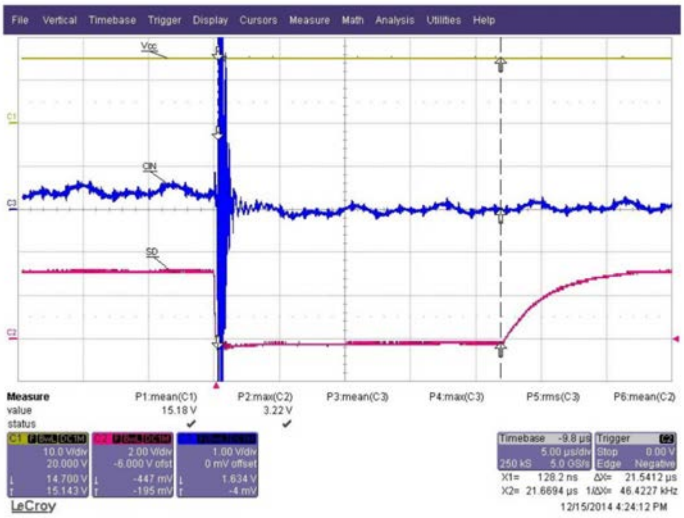


Figure 11. SD failure due to undervoltage (UVLO below 70 µs) shows the shutdown event as the result of an undervoltage condition on the V_{CC} supply. If V_{CC} drops below the undervoltage threshold, the shutdown can stop the application. If the voltage on V_{CC} rises above the V_{CC} on threshold in less than 70 µs, the SD event time is about 70 µs.

Figure 11. **SD failure due to undervoltage (UVLO below 70 µs)**

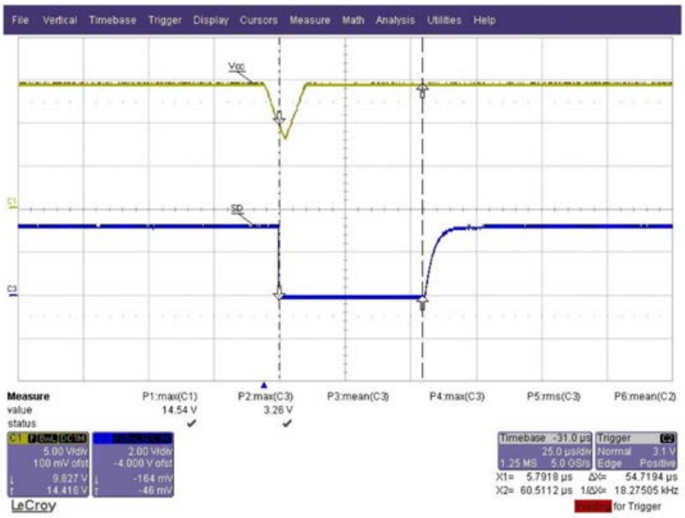
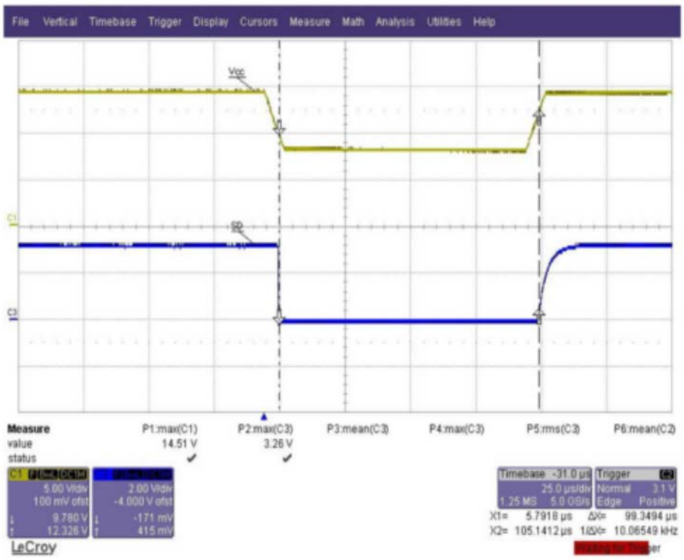


Figure 12. SD failure due to undervoltage (UVLO above 70 µs) shows the shutdown event as the result of an undervoltage condition on the V_{CC} supply. In this case, the drop on V_{CC} is greater than 70 µs. The SD event time is the same as the duration of drop.

Figure 12. SD failure due to undervoltage (UVLO above 70 µs)



4.3.3 Shunt resistor selection

The value of the shunt resistor is calculated by the following equation:

$$R_{SH} = \frac{V_{ref}}{I_{OC}} \tag{1}$$

Where V$_{ref}$is the internal comparator (CIN) (0.51 V typ.) and I$_{OC}$ is the current of overcurrent detection level. The maximum value of overcurrent protection level should be set less than the pulsed collector current in the datasheet. In this design the over current threshold level is fixed @ I$_{OC}$= 9.1 A.

$$R_{SH} = \frac{V_{ref} \cdot \left(\frac{R23 + R53}{R53}\right) + V_F}{I_{OC}} = \frac{0.51 \cdot \left(\frac{1000 + 4700}{4700}\right) + 0.18}{9.1} = 0.0877\Omega \tag{2}$$

Where V$_F$ is the voltage drop across diodes D3, D4 and D5.

The commercial value chosen was 0.08 Ω to which corresponds a level of 9.8 A.

The power rating of the shunt resistor is calculated by the following equation:

$$P_{SH} = \frac{1}{2} \cdot \frac{I_{load(\max)}^2 \cdot R_{SH} \cdot margin}{Deratingratio} \tag{3}$$

Where:

- I$_{load(max)}$: Maximum load current of inverter
- R$_{SH}$: Shunt resistor value at Tc=25°C
- Derating ratio: Power derating ratio of shunt resistor @ 100°C
- Margin: Safety margin of 30%

I$_{load(max)}$ is calculated considering the RMS value of the IPM nominal current including a safety margin.

$$I_{load(\max)} = \frac{I_{nom(@80°C)}}{\sqrt{2}} * 0.85 = 4.2A_{rms} \tag{4}$$

Power shunt value is:

$$P_{SH} = \frac{1}{2} \cdot \frac{4.2^2 \cdot 0.08 \cdot 1.3}{0.8} = 1.157W \tag{5}$$

Considering the commercial value, 2W shunt resistor was selected.

Based on the previous equations and conditions, minimum shunt resistance and power rating is summarized in Section 4.3.3 table.

Table 2. **Shunt selection**

Device	$OCP_{(peak)}$ [A]	$I_{load(max)}$ [Arms]	R_{SHUNT} [Ω]	Shunt power rating P_{SH} [W]
STIB1060DM2T-L	9.8	4.2	0.08	2

4.3.4 RC filter

An RC filter network is required to prevent undesired short circuit operation due to the noise on the shunt resistor. In this design, the RC filter, composed of R23, R18, R21, R24 and C19, has a constant time of about 1.3 µs. Adding the turn-off propagation delay of the gate driver and the MOSFET turn-off time (hundreds of nanoseconds in total), the total delay time is less than 5 µs of short circuit withstand MOSFET time.

4.3.5 Single- or three-shunt selection

Single- or three-shunt resistor circuits can be adopted by setting the solder bridges SW5, SW6, SW7 and SW8.

The figures below illustrate how to set up the two configurations.

Figure 13. **One-shunt configuration**

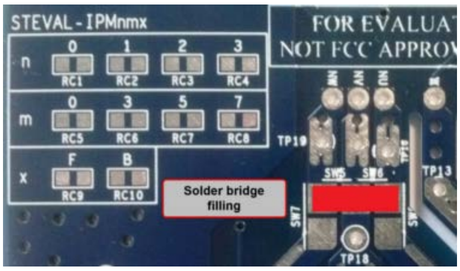
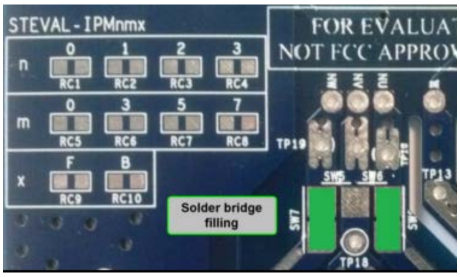


Figure 14. **Three-shunt configuration**



5 Current sensing amplifying network

The STEVAL-IPMM10B motor control demonstration board can be configured to run in three-shunt or single-shunt configurations for field oriented control (FOC).

The current can be sensed thanks to the shunt resistor and amplified by using the on board operational amplifiers or by the MCU (if equipped with op-amp).

Once the shunt configuration is chosen by setting solder bridge on SW5, SW6, SW7 and SW8 (as described in Section 4.3.5 Single- or three-shunt selection), the user can choose to send the voltage shunt to the MCU amplified or unamplified.

Single-shunt configuration requires a single op amp and three-shunt configuration requires three op amps; therefore, in single-shunt configuration, the only voltage which is sent to the MCU to control the sensing is connected to phase V through SW2.

SW1, SW2, SW4 can select which signals are sent to micro, as described below:

Table 3. **Op-amp sensing configuration**

Symbol	Configuration	Bridge	Sensing
SW1	Single Shunt	1-2	open
		2-3	open
	Three Shunt	1-2	On-board op-amp
		2-3	MCU op-amp
SW2	Single Shunt	1-2	On-board op-amp
		2-3	MCU op-amp
	Three Shunt	1-2	On-board op-amp
		2-3	MCU op-amp
SW4	Single Shunt	1-2	open
		2-3	open
	Three Shunt	1-2	On-board op-amp
		2-3	MCU op-amp

The operational amplifier TSV994 used on amplifying networks has a 20 MHz gain bandwidth and operates with a single positive supply of 3.3 V.

The amplification network must allow bidirectional current sensing, so that an output offset VO = +1.65 V represents zero current.

Referencing the STIB1060DM2T-L (IOCP = 9.8 A; RSHUNT = 0.08 Ω), the maximum measurable phase current, considering that the output swings from +1.65 V to +3.3 V (MCU supply voltage) for positive currents and from +1.65 V to 0 for negative currents is:

$$MaxMeasCurrent = \frac{\Delta V}{r_m} = 9.8A \tag{6}$$

$$r_m = \frac{\Delta V}{MaxMeasCurrent} = \frac{1.65}{9.8} = 0.168\Omega \tag{7}$$

The overall trans-resistance of the two-port network is:

$$r_m = R_{SHUNT} \cdot AMP = 0.08 \cdot AMP = 0.168\Omega \tag{8}$$

(9)

$$AMP = \frac{r_m}{R_{SHUNT}} = \frac{0.168}{0.08} = 2.1$$

Finally choosing R_a=R_b and R_c=R_d, the differential gain of the circuit is:

$$AMP = \frac{R_c}{R_a} = 2.1 \tag{10}$$

An amplification gain of 2.1 was chosen. The same amplification is obtained for all the other devices, taking into account the OCP current and the shunt resistance, as described in Table 1.

The RC filter for output amplification is designed to have a time constant that matches noise parameters in the range of 1.5 µs:

$$4 \cdot \iota = 4 \cdot R_e \cdot C_c = 1.5\mu s \tag{11}$$

$$C_c = \frac{1.5\mu s}{4 \cdot 1000} = 375pF\left(330pF selected\right) \tag{12}$$

Table 4. **Amplifying networks**

Phase	Amplifying network				RC filter	
	R_a	R_b	R_c	R_d	R_e	C_c
Phase U	R30	R32	R29	R33	R31	C25
Phase V	R35	R37	R34	R39	R36	C29
Phase W	R40	R42	R38	R43	R41	C31

6 Temperature monitoring

The SLLIMM 2nd series family integrates a temperature sensor (VTSO) on the low side gate driver and an NTC thermistor placed close to the power stage.

They can be selected via SW3.

The board is designed to use both of them to monitor the internal IPM temperature through the MCU.

6.1 Thermal sensor (VTSO)

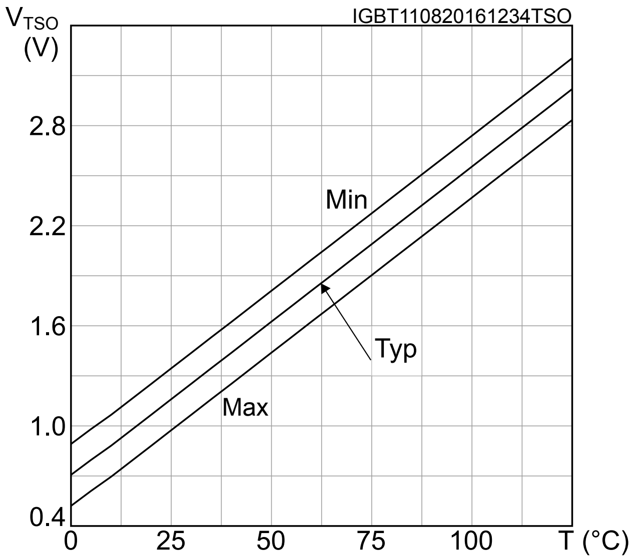
A voltage proportional to the temperature is available on the TSO pin (17) and easily measurable on the TP20 test pin.

To improve noise immunity, a 1 nF (C16) capacitor filter is placed on this pin.

The thermal sensor does not need any pull down resistors.

The following graph shows typical voltage variation as a function of temperature.

Figure 15. **Thermal sensor voltage vs temperature**



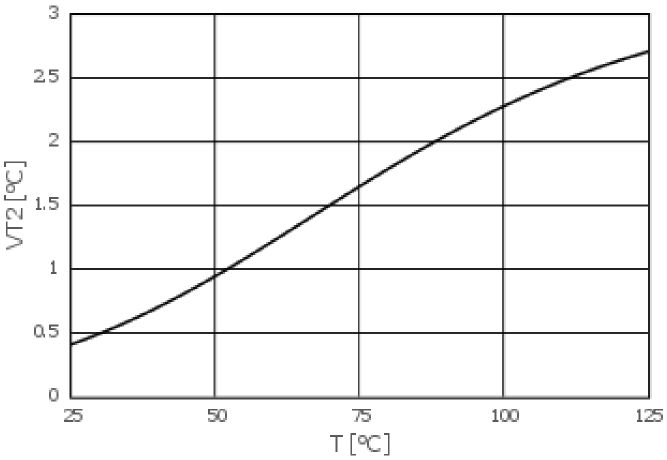
6.2 NTC Thermistor

The embedded thermistor (85 kΩ at 25 °C) in the IPM is connected between pins T1 and T2 (26, 25).

A12 kΩ pull down resistor (R10) ensures that the voltage variation on the NTC as a function of temperature is almost linear. This voltage is easily monitored on TP1 test pin.

The figure below shows the typical voltage on T2 as function of temperature.

Figure 16. NTC voltage vs temperature



7 Firmware configuration for STM32 PMSM FOC SDK

The following table summarizes the parameters which customize the latest version of the ST FW motor control library for permanent magnet synchronous motor (PMSM): STM32 PMSM FOC SDK for this STEVAL-IPMM10B.

Table 5. **ST motor control workbench GUI parameters**

Block	Parameter	Value
Over current protection	Comparator threshold	(13) $V_{ref} \cdot \left(\frac{R23 + R53}{R53}\right) + V_F = 0.8V$
	Overcurrent network offset	0
	Overcurrent network gain	Comparator threshold (see equation) / Iocp (see Section 4.3.3 Shunt resistor selection)
Bus voltage sensing	Bus voltage divider	1/125
Rated bus voltage info	Min rated voltage	125 V
	Max rated voltage	400 V
	Nominal voltage	325 V
Current sensing	Current reading typology	Single- or three-shunt
	Shunt resistor value	See shunt value in Section 4.3.3 Shunt resistor selection
	Amplifying network gain	2.1
Command stage	Phase U Driver	HS and LS: Active high
	Phase V Driver	HS and LS: Active high
	Phase W Driver	HS and LS: Active high

8 Connectors, jumpers and test pins

Table 6. **Connectors**

Connector	Description/pinout	
J2	Motor control connector	
	1 - emergency stop	2 - GND
	3 - PWM-1H	4 - GND
	5 - PWM-1L	6 - GND
	7 - PWM-2H	8 - GND
	9 - PWM-2L	10 - GND
	11 - PWM-3H	12 - GND
	13 - PWM-3L	14 - HV bus voltage
	15 - current phase A	16 - GND
	17 - current phase B	18 - GND
	19 - current phase C	20 - GND
	21 - NTC bypass relay	22 - GND
	23 - dissipative brake PWM	24 - GND
	25 - +V power	26 - heat sink temperature
	27- PFC sync.	28 - VDD_m
	29 - PWM VREF	30 - GND
	31 - measure phase A	32 - GND
	33 - measure phase B	34 - measure phase C
J3	Motor connector • phase A • phase B • phase C	
J4	VCC supply (20 VDC max) • positive • negative	
J5	Hall sensors / encoder input connector 1. Hall sensors input 1 / encoder A+ 2. Hall sensors input 2 / encoder B+ 3. Hall sensors input 3 / encoder Z+ 4. 3.3 or 5 Vdc 5. GND	
J7	Supply connector (DC – 125V to 400 V) 1. + (positive terminal) 2. - (negative terminal)	

Table 7. **Jumpers**

Jumper	Description
SW3	TSO/NTC
	TSO: jumper on 1-2
	NTC: jumper on 2-3

Jumper	Description	
SW1	To choose current U to send to control board:	
	Jumper on 1-2: from amplification	
	Jumper on 2-3: directly from motor output	
SW2	To choose current V to send to control board	
	Jumper on 1-2: from amplification	
	Jumper on 2-3: directly from motor output	
SW4	To choose current W to send to control board:	
	Jumper on 1-2: from amplification	
	Jumper on 2-3: directly from motor output	
SW13	To modify phase A hall sensor network	
SW14	To modify phase B hall sensor network	
SW15	To modify phase C hall sensor network	
SW9, SW16	To choose input power for Hall/Encoder	
	Jumper on 1-2: 5 V	
	Jumper on 2-3: 3.3 V	
SW5, SW6SW7, SW8	To choose one-shunt or three-shunt configuration. (Through solder bridge)	
	SW5, SW6 closed SW7, SW8 open	one shunt
	SW5, SW6 open SW7, SW8 closed	three shunt

Table 8. **Test pins**

Test pin	Description
TP1	NTC (T2 pin)
TP2	VBOOTw
TP3	VBOOTv
TP4	VBOOTu
TP5	HinU (high side U control signal input)
TP6	HinV (high side V control signal input)
TP7	HinW (high side W control signal input)
TP8	VCCH
TP9	phase A (U pin)
TP10	phase B (V pin)
TP11	Ground
TP12	LinU (high side U control signal input)
TP13	phase C (W pin)
TP14	LinV (high side V control signal input)
TP15	LinW (high side W control signal input)
TP16	Negative DC input for U phase
TP17	CIN

Test pin	Description
TP18	Negative DC input for V phase
TP19	Negative DC input for W phase
TP20	TSO (TSO pin)
TP21	Ground
TP22	Ground
TP23	SD (shutdown pin)
TP24	Current_A_amp
TP25	Current_B_amp
TP26	Current_C_amp

9 Bill of material

Table 9. **STEVAL-IPMM10B bill of materials**

Item	Q.ty	Ref.	Part/Value	Description	Manuf.	Order code
1	4	C2, C22, C26, C28	10 nF, 50V, ±10%	Ceramic Multilayer Capacitors, SMD 1206	AVX	12065C103KAT2A
2	9	C10, C11, C14, C15, C17, C18, C35, C36, C37	10 pF, 100V, ±10%	Ceramic Multilayer Capacitors, SMD 1206	AVX	12061A100JAT2A
3	4	C20, C25, C29, C31	330 pF, 50V, ±10%	Ceramic Multilayer Capacitors, SMD 1206	AVX	12065A331JAT2A
4	3	C5, C6, C7	2.2 µF, 25V, ±10%	Ceramic Multilayer Capacitors, SMD 1206	Murata	GCM31MR71E225KA57L
5	6	C8, C13, C23, C32, C33, C34	100 nF, 50V, ±10%	Ceramic Multilayer Capacitors, SMD 1206	AVX	12065C104KAZ2A
6	2	C12, C21	4.7 µF, 50V, ±20%	Electrolytic Capacitor, 4x4	any	any
7	2	C19, C16	1 nF, 50V, ±10%	Ceramic Multilayer Capacitors, SMD 1206	Kemet	C1206C102K5RACTU
8	1	C9	0.1 µF, 630V, ±10%	Ceramic Multilayer Capacitors, SMD 1812	Murata	GRM43DR72J104KW01L
9	3	C24, C27, C30	100 pF, 100V, ±10%	Ceramic Multilayer Capacitors, SMD 1206	Kemet	C1206C101J1GACTU
10	2	C3, C4	47 µF, 50V, ±20%	Electrolytic Capacitor, 4x4	any	any
11	5	D1, D3, D4, D5 D6	-	Schottky Diode, SOD323	ST	BAT48J
12	1	D2	Red	LED 3 mm, 2 mA, universal	Ledtech	L4RR3000G1EP4
13	1	J2	34 pins	445-6043-2-ND connector 34-pins	RS	625-7347
14	1	J3	7.5 mm - 3P, 400V	connector	TE Connectivity AMP Connectors	282845-3
15	1	J4	5 mm - 2P, 50V	connector	Phoenix Contact	1935161
16	1	J1	7.5 mm - 2P, 300V	connector	On Shore Technology Inc	OSTVI024152

Item	Q.ty	Ref.	Part/Value	Description	Manuf.	Order code
17	1	J5	2.54 mm - 5P, 63V	Five pins of pin header	RS	W81136T3825RC
18	2	R1, R2	470 kΩ, 400V, 1/4, ±1%	metal film resistor, SMD 1206	any	any
19	1	R4	7.5 kΩ, 400V, 1/4, ±1%	metal film resistor, SMD 1206	Panasonic	ERJP08F7501V
20	1	R3	120 Ω, 400V, 1/4, ±1%	metal film resistor, SMD 1206	any	any
21	3	R7, R13, R17	3.9 kΩ, 25V, 1/4, ±1%	metal film resistor, SMD 1206	any	any
22	18	R5, R6, R8, R9, R14, R15, R19, R20, R23, R30, R32, R31, R36, R35, R41, R42, R40, R37	1 kΩ, 25V, 1/4, ±1%	metal film resistor, SMD 1206	any	any
23	3	R11, R16, R22	3.3 kΩ, 25V, 1/4, ±1%	metal film resistor, SMD 1206	any	any
24	1	R28	10 kΩ, 25V, 1/4, ±1%	metal film resistor, SMD 1206	any	any
25	1	R10	12 kΩ, 25V, 1/4, ±1%	metal film resistor, SMD 1206	any	any
26	6	R29, R33, R34, R38, R39, R43	2.1 kΩ, 25V, 1/4, ±1%	metal film resistor, SMD 1206	any	any
27	1	R12	5.6 kΩ, 25V, 1/4, ±1%	metal film resistor, SMD 1206	any	any
28	3	R25, R26, R27	0,08 Ω, 2	metal film resistor, SMD 2816	Vishay / Dale	WSL2816R0800FEH
29	7	R44, R45, R46, R50, R51, R52, R53	4.7 kΩ, 25V, 1/4, ±1%	metal film resistor, SMD 1206	any	any
30	3	R47, R48, R49	2.4 kΩ, 25V, 1/4, ±1%	metal film resistor, SMD 1206	any	any
31	6	SW1, SW2, SW3, SW4, SW9, SW16	Jumper 2.54	Three pins of pin header	RS	W81136T3825RC
32	6	SW10, SW11, SW12, SW13, SW14, SW15	Jumper 2.54	Two pins of pin header	RS	W81136T3825RC
33	12	-	2.54mm	low profile connector	RS	881545-2
34	42	SW7, SW8	-	Solder Bridge	-	-
35	2	SW5, SW6	open	-	-	-

Item	Q.ty	Ref.	Part/Value	Description	Manuf.	Order code
36	26	TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP18, TP19, TP20, TP21, TP22, TP23, TP24, TP25, TP26	PCB terminal 1mm	Test pin	KEYSTONE	5001
37	1	U1	3-phase inverter, 12.5A, 600 V Power MOSFET	Op amp, SO14	ST	TSV994IDT
38	1	U2	-	SDIP2B-26L type L1	ST	STIB1060DM2T-L
39	4	RC1, RC5, RC8, RC13	0 Ω, ANY, ANY, ±ANY%	SMD 0805	ANY	ANY
40	9	RC2, RC3, RC4, RC6, RC7, RC9, RC10, RC11, RC12	-	-	-	-
41	9	to close swith for: SW1, SW2, SW3, SW4, SW9, SW10, SW11, SW12, SW16	-	Female Straight Black Handle, Open Top 2 Way 1 Row 2.54mm Pitch	TE Connectivity	1-881545-1
42	1	PCB	100.3x121.4x1.6mm	100.3x121.4x1.6mm-2 Layer-CU thikness 105micron	-	-

10 PCB design guide

Optimization of PCB layout for high voltage, high current and high switching frequency applications is a critical point. PCB layout is a complex matter as it includes several aspects, such as length and width of track and circuitareas, but also the proper routing of the traces and the optimized reciprocal arrangement of the various system elements in the PCB area.

A good layout can help the application to properly function and achieve expected performance. On the otherhand, a PCB without a careful layout can generate EMI issues, provide overvoltage spikes due to parasitic inductance along the PCB traces and produce higher power loss and even malfunction in the control and sensing stages.

In general, these conditions were applied during the design of the board:

- PCB traces designed as short as possible and the area of the circuit (power or signal) minimized to avoid the sensitivity of such structures to surrounding noise
- Good distance between switching lines with high voltage transitions and the signal line sensitive to electrical noise
- The shunt resistors were placed as close as possible to the low side pins of the SLLIMM. To decrease the parasitic inductance, a low inductance type resistor (SMD) was used
- RC filters were placed as close as possible to the SLLIMM pins in order to increase their efficiency

10.1 Layout of reference board

All the components are inserted on the top of the board. Only the IPM module is inserted on the bottom to allow the insertion of a suitable heatsink for the application.

Figure 17. Silk screen and etch - top side

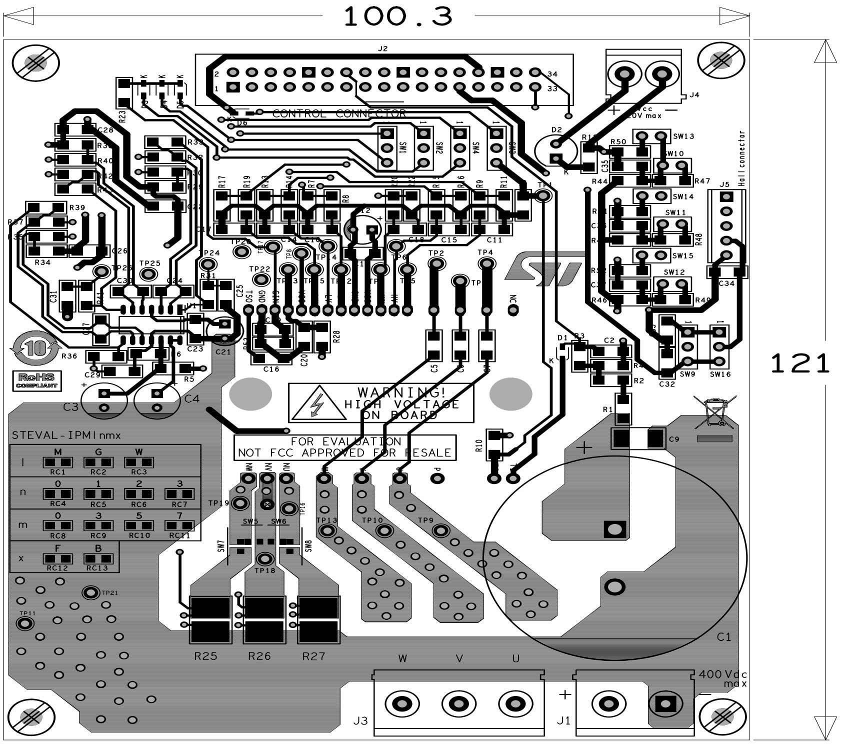
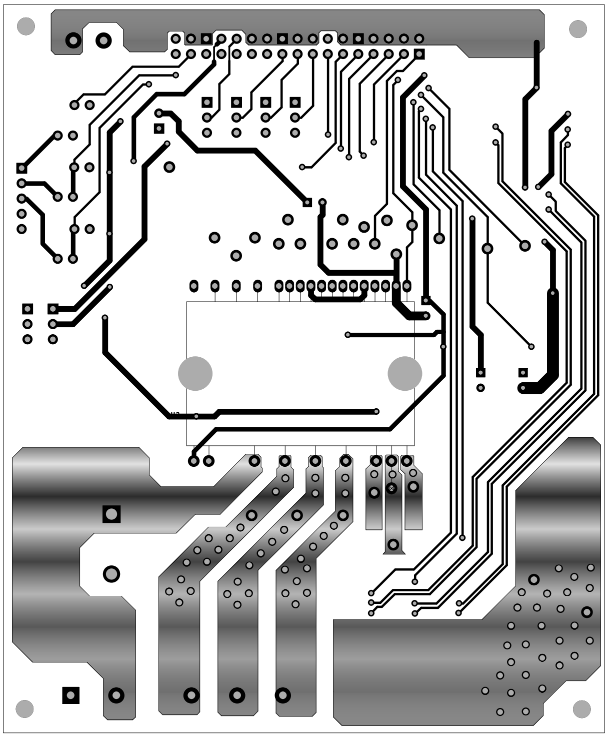


Figure 18. Silk screen and etch - bottom side



11 Recommendations and suggestions

- The BOM list is not provided with a bulk capacitor already inserted in the PCB. However, the necessary space has been included (C1). In order to obtain a stable supply voltage, according to the application conditions and current ripple requirements, it's advisable to use an adequate bulk capacitor. For general motor control applications, an electrolytic capacitor of at least 100 µF is suggested
- Similary, the PCB does not come with an heat sink, it can be placed above the IPM on the back of the PCB with thermal conductive foil and screws. Heat sink R_{TH} value is an important factor for good thermal performance and depends on certain factors such as current phase, switching frequency, power factor and ambient temperature. For an adequate heat sink dimensioning, it is suggest to use ST PowerStudio software (STSW-POWERSTUDIO), available on www.st.com.
- The board requires +5 V and +3.3 V to be supplied externally through the 34-pin motor control connector J2. Please refer to the relevant board manuals for information on key connections and supplies.

12 General safety instructions

Danger:

The evaluation board works with high voltage which could be deadly for the users. Furthermore all circuits on the board are not isolated from the line input. Due to the high power density, the components on the board as well as the heat sink can be heated to a very high temperature, which can cause a burning risk when touched directly. This board is intended for use by experienced power electronics professionals who understand the precautions that must be taken to ensure that no danger or risk may occur while operating this board.

Caution: After the operation of the evaluation board, the bulk capacitor C1 (if used) may still store a high energy for several minutes. So it must be first discharged before any direct touching of the board.

Important:

To protect the bulk capacitor C1, we strongly recommended using an external brake chopper after C1 (to discharge the high brake current back from the induction motor).

Revision history

Table 10. **Document revision history**

Date	Version	Changes
16-Apr-2020	1	Initial release.

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